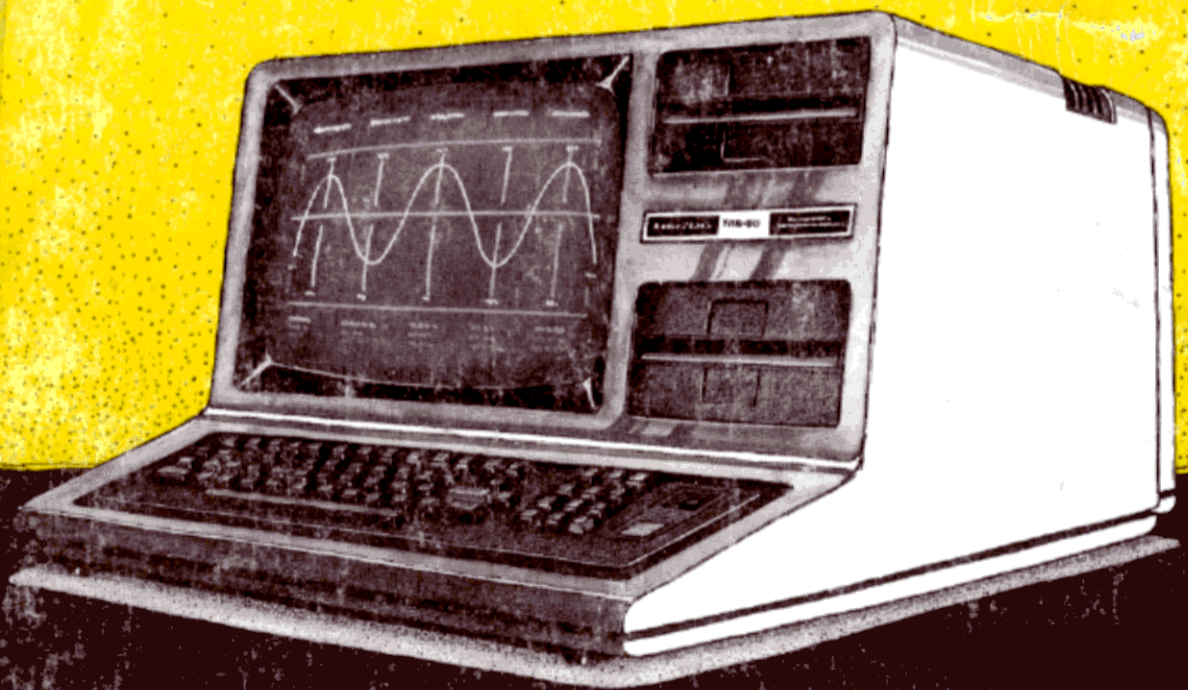


TRS-80® Model III

Technical Reference Manual

For programmers
and technicians



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IMPORTANT NOTICE

This Technical Reference Manual is written for owners of the TRS-80 Model III Computer, who have a thorough understanding of electronics and computer circuitry. It is not written to the beginner's level of comprehension.

This manual contains detailed schematics and theories of operation for each major part of the Model III. These tools will aid you with designing interfaces for your computer, repairing your own computer after its warranty has expired, or simply obtaining practical knowledge of your TRS-80 Model III operation.

Radio Shack will not be liable for any damage caused, or alleged to be caused, by the customer or any other person using this technical manual to repair, modify, or alter the TRS-80 Model III Computer in any manner.

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SECTION I

INTRODUCTION

SYSTEM OVERVIEW

The Radio Shack TRS-80 Model III Microcomputer is an enhanced version of Radio Shack's popular TRS-80 Microcomputer (Model I). The TRS-80 Model III is software compatible with the Model I so that owners of either system can take advantage of the large number of programs available.

Features of the TRS-80 Model III which are common to the TRS-80 Model I include:

- Availability of Level I or Level II BASIC in ROM
- Full size typewriter style keyboard
- A 12-inch video display
- Built-in cassette interface
- Character display of 16 lines of 64 characters
- Graphics under control of BASIC (128 H x 48 V)
- UL recognized construction

In addition, the Model III has the following standard features:

- 12-key numeric keypad for rapid entry of numbers
- Rugged cabinet housing keyboard, electronics, video display, and power supply
- Direct drive video monitor for improved resolution
- Internal power supply
- Parallel printer port for use with Radio Shack printers

Several other features are available when Level II BASIC is used; features such as: real time clock, upper and lower case characters, RAM internally expandable to 48K bytes, I/O port for peripheral expansion, and cassette interface available with 500 and 1500 baud rates.

Optional peripherals for the TRS-80 Model III include disk drives (two built-in, two external) with double density for increased storage capacity, and a built-in RS-232 serial interface for communications and peripheral interface.

The Block Diagram shows the various internal components and connections of the Model III Microcomputer.

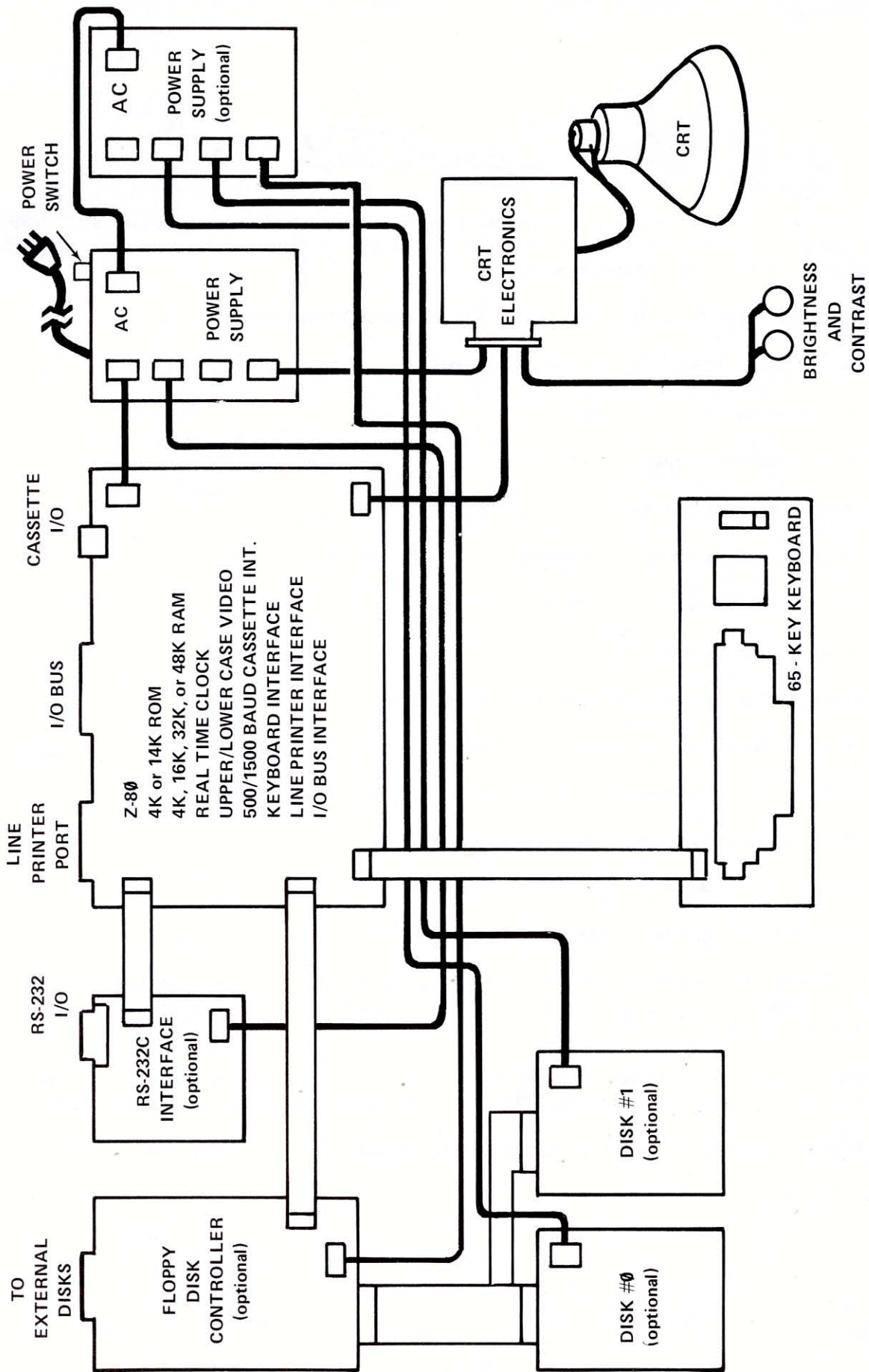


FIGURE 1. TRS-80 MODEL III BLOCK DIAGRAM

SECTION II

DISASSEMBLY/REASSEMBLY

DISASSEMBLY

CASE:

1. Remove all cables from the bottom and rear of the Computer. Position the Computer on its rear panel to provide easy access to the case bottom. Remove the ten screws from the case bottom. Notice the different types and lengths of screws and note their positions. Set them aside in groups.
2. Position the Computer upright and remove the #6 screw and washer from the top of the back panel of the case.
3. Very carefully remove case top, lifting **straight up** and setting it aside to the left (if facing video screen). Be careful not to exceed the length of the video cable.
4. Remove screws from the chassis shield and the ground connectors and remove the shield. **

CPU BOARD:

1. Remove all cables connecting the CPU Board (power supply cable, video, keyboard, and cassette cables, and if applicable, the RS-232 and FDC inter-connect cables).
2. Remove the five screws fastening the PC Board (two in upper right corner, three on bottom).
3. Remove the small PCB Mount Bracket and its two screws from atop the metal chassis bracket. **
4. Make sure all cables to the CPU Board have been disconnected then remove the Board. (If your unit uses plastic spacer mounts to hold the Board, press the small tabs on the mounts through the mounting holes in the PCB and gently pull the CPU Board off.)

FDC BOARD (optional):

NOTE: The CPU Board must be removed before removing the FDC Board.

1. Be sure to disconnect all cables to the FDC Board.
2. Remove the screws holding the FDC Board to the metal chassis and remove the Board.

RS-232 BOARD (optional):

NOTE: The CPU Board must be removed before removing the RS-232 Board.

1. Be sure to remove all cables connecting the RS-232 Board.
2. Remove the screws connecting the PC Board to the chassis and remove the Board.

MAIN POWER SUPPLY:

1. Remove all interconnect cables to the Boards fastened on the metal chassis bracket (power supply cable, video, keyboard, and cassette cables, and if applicable, RS-232 and FDC power connectors and the Disk ribbon cable).
2. Remove the four screws fastening the metal chassis bracket to the case bottom.
3. Make sure all inter-connecting cables are removed, then carefully lift out chassis bracket and attached Boards.
4. Remove the four screws fastening the Power Supply to the Bracket (notice where the ground tab is fastened), then carefully remove the power supply.

DISK DRIVE POWER SUPPLY (optional):

1. Disconnect all cables and wires connecting to the Power Supply.
2. Remove the four screws fastening the Board to the Disk Mounting Bracket (notice where the ground tab is fastened), then carefully remove the Power Supply.

DISK DRIVES (optional):

1. To remove the Disk Drive in the top position, carefully remove the FDC inter-connect cable connected to the rear of the Drive.
2. Remove the four screws and washers (two on each side) which connect the Drive to the Disk Mounting Bracket.
3. Disconnect the power supply connector from the bottom of the top board in the Disk Drive and also remove the ground wire from the rear of the Drive.

**Not applicable to all units.

4. To remove the Disk Drive in the bottom position, **you must first remove the Disk Drive Power Supply.**
5. After removing the Power Supply, remove the FDC inter-connect cable from the rear of the Drive.
6. Remove the four screws and washers (two on each side) which connect the Drive to the Disk Mounting Bracket.
7. Disconnect the power supply connector from the bottom of the top board in the Disk Drive and also remove the ground wire from the rear of the Drive.

VIDEO MONITOR (CRT) AND VIDEO BOARD

1. Disconnect the four color coded wires with spade lugs from the CRT yoke. (Be sure to note their positions.)
2. Disconnect the connector on the rear of the CRT neck.

WARNING

There may be a high voltage charge on the high voltage anode. To discharge, connect one end of a wire to a known good ground and connect the other end of the wire to the blade of a common screwdriver. Insert the screwdriver blade under the suction cup and touch it to the clip holding the wire to the CRT.

3. Insert a common screwdriver under the suction cup on the high-voltage anode wire on the side of the CRT. Use the screwdriver to compress the clip holding the wire to the tube and pull the wire free.
4. Remove the ground wire fastened directly to the Video Board.
5. Remove the upper right and lower left nuts and washers which hold the CRT in place.

CAUTION

If dropped, the CRT may implode. To avoid this kind of accident, support the CRT while performing the next step.

6. Remove the remaining lower right and upper left nuts, and washers and carefully remove the CRT.
7. Disconnect the CPU cable connector from the Video Board.
8. Remove the two screws fastening the Video Board to the Case Top and carefully lift out Board.

REASSEMBLY

RS-232 BOARD (optional):

1. Install the PC Board using #6 x 3/8" screws. If applicable, press the PC Board onto the plastic spacer mounts then fasten with the screws.
2. Reconnect all cables to the RS-232 Board.

FDC BOARD (optional):

1. Install the PC Board using #6 x 3/8" screws and the plastic spacer mounts, if used.
2. Reconnect all cables to the FDC Board.

CPU BOARD:

1. Make sure good insulating washers are attached to the CPU Board (Rev. F boards only) then fasten the Board using #6 x 1/4" screws.
2. Reconnect all cables to the CPU Board (power supply cable, video, keyboard, and cassette cables, and if applicable, RS-232 and FDC inter-connect cables).
3. Attach the small PCB Mount Bracket (if used) to the metal chassis bracket with two #6 x 1/4" screws.

MAIN POWER SUPPLY:

1. Fasten the Power Supply to the metal chassis bracket using four #6 x 1/4" screws. Be sure the ground tab is fastened back in place.
2. Install the chassis bracket (with all Boards in place) in the case bottom using four #6 x 1/4" screws.
3. Reconnect all cables (power supply, video, keyboard, and cassette cables, and RS-232 and FDC power cables and Disk ribbon cable if necessary).

DISK DRIVE (optional):

1. Place the Disk Drive in the bottom position and reconnect the ground wire and power supply connector.
2. Fasten the Drive with four #6 x 1/2" screws and four flat washers (two on each side).
3. Reconnect the FDC inter-connect cable to the rear of the Drive.
4. Position the second Disk Drive in the top position and reconnect the ground wire and power supply connector.
5. Fasten with four screws and washers (two on each side).

6. Reconnect the FDC inter-connect cable to the rear of the Drive.

DISK DRIVE POWER SUPPLY (optional):

1. Before installing the Power Supply, be sure that the bottom Disk Drive is mounted in place and the Disk Shield is in position on the Disk Mounting Bracket.
2. Reconnect all cables and wires to the Power Supply.
3. Fasten the Power Supply with four #6 x 3/8" screws. Be sure the ground tab is fastened back in place.

VIDEO MONITOR (CRT) AND VIDEO BOARD:

1. Position the CRT in the Case Top and install the upper left and lower right #10 washers and nuts.
2. Install the upper right and lower left #10 washers and nuts. Be sure to reconnect the ground wire from the CPU cable. It will require two nuts to fasten it.
3. Install the Video Board into the Case and fasten with two #6 x 1/4" screws.
4. Connect the ground wire with solder lug back to the Video Board.
5. Install the plug on the rear of the CRT neck.
6. Install the four color coded wires with spade lugs to their associated terminals (as determined by a colored dot on the yoke near each terminal).
7. Install the high-voltage anode wire on the side of the CRT. Use a screwdriver to compress the clip and insert it into the CRT. Press down on the suction cup to secure.

CASE:

1. Double-check to be sure all wires are connected correctly and all Boards are properly fastened.
2. Attach the chassis shield (if used) with #6 x 1/4" screws and reconnect the ground connectors.
3. Carefully place the Case Top over the Case Bottom. **Do not hit the CRT neck. It could implode or break off.**
4. Install the #6 x 3/8" sheet metal screw and flat washer in the top rear panel of the Case.
5. Carefully rest the Computer on its rear panel and replace the ten #8 screws; five 1" sheet metal toward rear, three 7/8" machine head along front, and two 1" machine head in remaining positions.

SECTION III

CPU CIRCUIT BOARD

TECHNICAL DESCRIPTION

The technical description of the Model III Computer CPU circuit board will be broken down into nine sections. These are:

1. Processor
2. RAM
3. Address Decoding
4. Video
5. Video Sync Circuits
6. Keyboard
7. Cassette Interfaces
8. Line Printer and Real Time Clock
9. I/O Bus

This breakdown, which follows the partitioning of the schematic diagrams, will allow easy explanation and referencing.

VIDEO SYNC CIRCUITS

The video sync circuits are required to meet the pulse width and polarity requirements of the video monitor. It also allows adjustment in both the horizontal and vertical planes in discrete increments. The vertical sync pulse VSYNC is active low and approximately $693\mu\text{sec}$ in duration. The frame rate is either 50 or 60 Hertz. The horizontal rate is 15,840 Hz and the signal HSYNC is active high with a duration of approximately $8\mu\text{sec}$. The vertical plane adjustment covers a total of eight rows and is adjustable in increments of one row (R1, R2, R4). The horizontal plane adjustment increments by two characters for a total coverage of 16 character positions. Both adjustments are accomplished with the use of wired "AND" gates U22 and U38 (LS266).

PROCESSOR

The CPU chip is a Z-80 that runs at a clock speed of 2.02752 MHz. The CPU clock is derived by dividing the basic video clock (10.1376 MHz) by five. U62 performs this function

and the clock is non-symmetrical with a 40 percent high duty cycle. The clock signal PQC is run through an active pull-up and becomes PCLOCK which has a full 5-volt swing with fast rise and fall times. The reset switch, which is located on the keyboard, is ORed with power on reset (R7, C54, U15) to provide a System RESET* signal. The Reset pin on the Z-80 is driven by RESET*. The address lines are buffered by LS244's (U91, U92), the data lines by an LS245 (U90), and control lines buffered by an LS367 (U76). The buffered control lines are combined in U89 and U86 to form memory and I/O port controls (RD*, WR*, IN*, OUT*).

See the CPU Timing Diagram for exact time relationships. U75 is used to switch the data bus buffer during INTAK* cycle or any read operation (I/O or Memory). Whenever one of the ROMs is being accessed, the data bus buffer is disabled by U108 since the ROMs data lines are located on the CPU data bus. BUSRQ*, HALT*, BUSAK*, and RFSH* are not used. The Model III has three sockets for the ROMs (U104, U105, U106. They are 64K bit, 32K bit, and 16K bit ROMs respectively.

RAM

The RAM consists of an array of up to twenty-four 16K dynamic memory chips with damping resistors located on all address and control lines (RP1, RP2, RP3). Chips U7 to U14 are addressed at 4000 to 7FFF. U25 to U32 are addressed at 8000 to BFFF and U43 to U50 are addressed at C000 to FFFF. The memory data is interfaced to the data bus by two 8T26s (U63, U64). Normally the data is driven into the memory array. However, on a read cycle U19 switches the direction of the transceivers and drives memory data onto the data bus. The -5 volts required by the RAMs is supplied by a 3-terminal regulator (MC7905C) which takes -12 volts as its input. See the CPU Timing Diagram for the relationship between RAS*, MUX, CAS*.

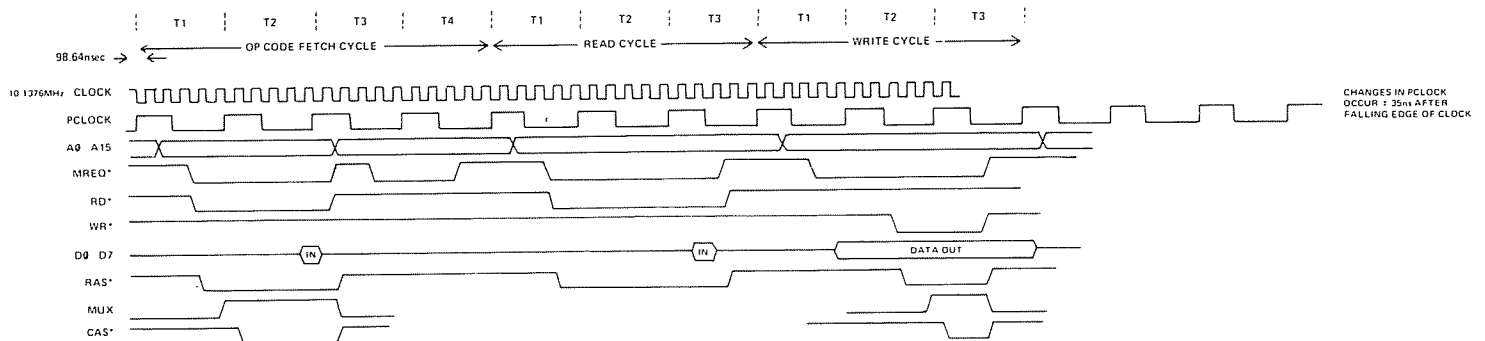


FIGURE 1. CPU TIMING DIAGRAM

ADDRESS DECODING

The Address Decoding provides all the selects for the system I/O ports, the ROMs, Keyboard, Video, and RAM memory control. Refer to the Memory Map for exact locations of devices.

The two LS138 demultiplexers provide the INPUT and OUTPUT strobes for system I/O ports E0 to FF; U41 for OUTs and U40 for INs. Memory timing consists of U37 and U61 in a shift register configuration clocked at 10.1376 MHz to give the correct relationship between RAS*, MUX, and CAS*.

MUX provides the switch between Row address and Column address on the address multiplexers U24 and U42 for the memory array. The three CAS signals are generated by LS139 (U58), LS32s (U59, U107) and one CAS for each row of RAMs.

Note that the first row of RAMs is the only one suitable for 4K RAMs (jumper option U to T, N to P, GG to FF). The ROM strobes (ROMA*, ROMB*, and ROMC*) are generated by the remaining section of the LS 139 (U58), and part of the LS 145 (U60).

The combinational logic below U60 (U75, U73, U72, U86) deletes two addresses from ROMC* (37E8 and 37E9) which correspond to the line printer address; thus, ROMCP* is the actual strobe going to the 16K bit ROM. The result is that the line printer may be accessed for a read as either a memory address (37E8) or an I/O port (F8). See the I/O ports and address space map. The remaining strobes KYBD* and VID* are also generated by the LS145 (U60).

MEMORY MAP OF MODEL III

| HEX ADDRESS | DESCRIPTION | DECIMAL SIZE (1K = 1024) |
|--------------|----------------|--------------------------|
| 0000 1FFF | ROM A | 8K |
| 2000 2FFF | ROM B | 4K |
| 3000 37FF | ROM C | 2K-2 |
| 37E8 37E9 | Printer Status | 2 |
| 3800 3BFF | Keyboard | 1K |
| 3C00 3FFF | Video | 1K |
| 4000 7FFF | RAM | 16K |
| 8000 BFFF | RAM | 16K |
| C000 FFFF | RAM | 16K |

I/O PORT DESCRIPTION

Name: LPIN*
 Port Address: 0F8H
 Access: Read Only
 Description: Read Line Printer Port Status

BIT 7 = BUSY
 1=True
 0=False

BIT 6 = OUTPAPER
 1=True
 0=False

BIT 5 = UNIT SELECT
 1=True
 0=False

BIT 4 = FAULT
 1=True
 0=False

Name: LPOUT*
 Port Address: 0F8H
 Access: Write Only
 Description: Line Printer Output Data Port

BIT 7 thru BIT 0 = ASCII Byte to be Printed.

Name: RTCIN*
 Port Address: 0E8H
 Access: Read Only
 Description: Clear Real Time Clock Interrupt

BIT 7 thru BIT 0 = Don't Care

Name: DISKOUT*
 Port Address: 0F0H to 0F3H
 Access: Write Only
 Description: Write to Disk Control Registers

Port 0F0H = Disk Command Register
 Port 0F1H = Disk Track Register
 Port 0F2H = Disk Sector Register
 Port 0F3H = Disk Data Register

Name: DISKIN*
 Port Address: 0F0H to 0F3H
 Access: Read Only
 Description: Read Disk Control Registers

Port 0F0H = Disk Status Register
 Port 0F1H = Disk Track Register
 Port 0F2H = Disk Sector Register
 Port 0F3H = Disk Data Register

Name: RS232IN*
 Port Address: 0E8H to 0EBH
 Access: Read Only
 Description: Read UART Registers

Port 0E8H = Modem Status
 Port 0E9H = N.A.
 Port 0EAH = UART Status Register
 Port 0EBH = UART Receiver Holding Register,
 Resets D.R.

Name: RS232OUT*
 Port Address: 0E8H to 0EBH
 Access: Write Only
 Description: UART Control, Data;
 Modem Control; BRG Control

Port 0E8H = UART Master Reset
 Port 0E9H = Baud Rate Register Load
 Port 0EAH = UART Control register and
 Modem Control
 Port 0EBH = UART Transmitter Holding Register

VIDEO

The Video section can be subdivided into four parts:

- A. Video RAM with associated addressing and data buffer
- B. Main oscillator and divider chain
- C. Character generation logic
- D. Wait logic

A. The video RAM consists of two 2114 static RAMs (U81, U82) which gives 1024 (1K) bytes of RAM. Addressing from the divider chain or the Z-80 CPU comes from the LS157 multiplexors (U69, U70, U71). The video data is buffered to the CPU data bus through an LS245 (U67), or to the character generator logic by the LS273 latch U68. Addressing control is determined by the signal RSVID* which is described in paragraph D.

B. The main oscillator consists of inverters from U2, crystal Y1, and discretes R1, R5, and C1. The oscillator runs in the fundamental mode at a frequency of 10.1376 MHz. This basic frequency is divided by two in U3 and becomes CLOCK/2. The CLOCK and CLOCK/2 signals are fed to mux U4 which provides the divider chain with the CHAIN signal (633.6 kHz) provides the shift register U52 with the SHIFT signal, and also supplies the signal LATCH (1/8 the rate of SHIFT) to various parts. MODSEL selects either the 64 character or 32 character mode. (Refer to the Video Timing diagram.) The main divider chain consists of two LS393s (U20, U56) and one LS74 (U1). This divider chain, connected as one long ripple counter, presents the character count, the line and row count, and the horizontal and vertical drive signals to

the rest of the video section. The horizontal drive signal (HDRV) runs at 15.840 kHz and results in 80 characters per line; 64 displayed and 16 blanked. The line count (L1 to L8) runs modulo 12 (i.e., twelve horizontal lines per character block). The row counter (R1 to R8 and VDRV) runs modulo 22 (60 Hz), or modulo 26 (50 Hz) depending which jumper option, "A", or "B" or "C", has been selected.

C. The character generation logic consists of a latch (LS273-U68) to hold the ASCII data, a ROM which contains the dot pattern making up the characters, a shift register (LS166 - U52) which serializes the 8-bit data for display on the screen, and the associated timing and control signals provided by the divider chain and oscillator circuits. On the rising edge of LATCH the LS273 stores the ASCII byte from the video RAMs. This data is presented to the character generator ROM to form part of the address of the character to be displayed. The other addressing information comes from the divider chain (L1 to L4) to select the scan line of the character to be displayed. (There are twelve scan lines in each character block.) On the next LATCH pulse the data from the ROM is latched into the shift register and shifted out by the SHIFT clock. The SHIFT clock runs eight times faster than LATCH, hence there are eight horizontal dots per character line. The LATCH signal into the shift register is qualified by DLYBLANK so that during horizontal retrace, vertical retrace, and the last four scan lines of each character displayed, the shift register will shift out zeros.

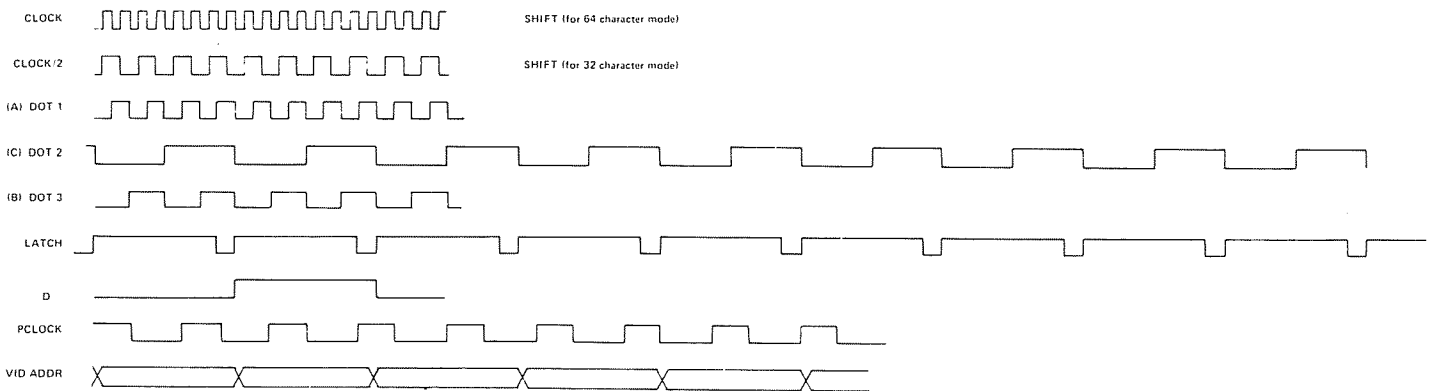


FIGURE 2. VIDEO TIMING DIAGRAM

If VD7 is a one and VD6 is a zero, then a graphics character will be displayed which uses LS153 (U54) and LS244 (U53) to load the data into the shift register. Note that both U36 and U53 are tri-state devices and that the enables for these devices (DLYCHAR* and DLYGRAPHIC*) are the complements of each other. This means that either character data or graphics data will be loaded into the shift register depending of course on the state of VD7 and VD6. The signal ENALTSET and an LS00 (U37) allow the 64 characters that are masked by the graphics characters to be displayed from the ROM (U36). When ENALTSET is a one, the 64 standard characters are displayed. When ENALTSET is a zero, 64 alternate characters are displayed.

- D. The wait logic forces the CPU into a wait state if the BLANK* signal is not present. This allows video RAM updates only during horizontal retrace, vertical retrace, and the blanking on the last four scan lines of a character since these are the conditions that form BLANK*. This will eliminate virtually all the "hashing" on the display. The logic consists of U17, U16, U18, U57, U39, and U1. When VID* is true, indicating the CPU wants access to the video RAM, and PBLANK* is false, both signals are combined in U16 to give PWAIT*. If PBLANK* is true, it is combined with VID* to give RSVID*, which is then granted access to the video RAM. This feature can be disabled through the DISWAIT input to U39 which is under software control.

KEYBOARD

The keyboard interface consists of open collector drivers (LS05) U34 and U35 which feed the 8 by 8 key matrix with addresses A0 through A7. The output of the matrix has the pullup resistors and CMOS receivers which give reliable key closure sensing even with key switches of up to 300 ohm resistance. The data from the CMOS buffer is driven onto the data bus by the LS240 (U66). The signal KYBD* strobes the octal data bus driver. The reset switch is also mounted on the keyboard assembly and the three lines required are routed in the twenty-pin keyboard cable to the reset circuit. Note that all electronic parts are mounted on the CPU Board; none are required on the PCB for the keyboard.

CASSETTE INTERFACE

There are two separate cassette circuits for 500 Baud and 1500 Baud. The 500 Baud Read circuitry is very similar in principle to the Read circuitry on Model I. The MC1741 forms a two pole high pass active filter to filter out 60 Hz noise. The two amplifiers of the MC1458 (U80) form a full-wave active rectifier. Capacitor C94 acts to smooth out the rectified output which is then fed to a 339 comparator (U96). Resistors R48, R49, and R51 provide a fixed threshold of 0.5V at pin 5 of U96. This gives a minimum level with which

the input signal at pin 4 may be compared against. Capacitor C93 provides a voltage equal to the average signal level, with R46 and CR9 providing fast charge and R48 providing a slow discharge. Capacitor C93 provides an equivalent AGC action since the comparator threshold becomes proportional to the signal level. The comparator outputs negative pulses corresponding to the input pulses which are then inverted by U2 and fed into the clock of a "D" flip-flop (U3). The "D" flip-flop will then be set and will stay set until cleared by CAS OUT* (equivalent to OUTSIG in Model I). CAS IN* will read the data stored in U3 and output it at pin 7 of the data bus.

The 500 Baud Write circuitry is identical to the write circuitry used in the Model I. This circuit is also used to provide the squarewave data for 1500 Baud. Data 00H gives 0.4V out, Data 01H gives 0.8V out, and Data 02H gives 0.0V out. The 1500 Baud uses 01H and 02H only. The 500 Baud output is a 250µsec pulse while the 1500 Baud output is a squarewave that varies in frequency between 1320 Hz and 2680 Hz.

The 1500 Baud cassette input consists of a zero crossing detector using U96. Diode CR8 is used to prevent the input signal from driving pin 10 of U96 negative. The output, pin 13 of U96, is normally high when the signal is applied and will provide a 50mV threshold at pin 11. R57 and R59 provide this 50mV of threshold and hysteresis. The output of the comparator is fed to the two 74LS74 "D" flip-flops which determine whether the rising or falling edge is detected and is also used to set an interrupt signal INT* using U18 and U35. ENCASINTF, pin 2, enables the falling edge interrupt latch and ENCASINTR, pin 12, enables the rising edge interrupt latch. Only one of the latches are enabled at any one time. CASIN* clears the interrupt latches and RDINT-STATUS* is used to read the data from the interrupt latch to tell which latch has been set. The cassette motor on relay is driven by U97.

LINE PRINTER AND REAL TIME CLOCK

The LS273 (U94) latches the data written to the Line Printer and the one-shot (U93) provides the data strobe. The printer status lines are buffered through the LS244 (U95). A full eight bits of data are buffered so that the Line Printer interface could be used for any general purpose parallel interface.

The Real Time Clock circuit provides either a 30 Hz or 25 Hz interrupt to the CPU if enabled. VDRV is divided by two at U83 (LS74) and latched in the other section of U83. This generates an interrupt through LS38 (U88) and the status can be read by strobing U84 (LS367) with RDINTSTATUS*. To clear the interrupt one must strobe RTCIN*.

IO BUS

The I/O Bus supports all the signals necessary to implement a device that is compatible with the Z-80's I/O structure. The LS245 (U101) buffers the data in both directions and is enabled by ENEXTIO. The direction is determined by LS244 (U102) and is also enabled by ENEXTIO. The control lines necessary for I/O operation are buffered by LS367 (U103) and they are also enabled also by ENEXTIO. External I/O waits and interrupts are also supported by the I/O bus via U87 and U88. Refer to the detailed I/O Bus description and timing diagram.

ADJUSTMENTS AND JUMPER POSITIONS

The jumper positions vary between 4K and 16K RAM models. Jumpers should be installed as described below.

| | |
|---------|--------------------------|
| 4K RAM | U to T, N to P, GG to FF |
| 16K RAM | S to T, R to P, EE to FF |

The CRT positioning jumpers also vary between the 50Hz and 60Hz models. Jumpers should be installed as described below. The Vertical and Horizontal Position jumpers are determined by the factory and depend on the frame rate and the monitor used.

The standard CRT jumper configurations for a 60 Hz computer are:

Vertical Frame Rate:

C to B

Vertical Position Adjustment:

D to E
K to L
J to H

Horizontal Position Adjustment:

V to W
CC to BB

The standard jumper configurations for a 50 Hz computer are as follows:

Vertical Frame Rate:

A to B

Vertical Position Adjustment:

D to E
M to L
G to H

Horizontal Position Adjustment:

V to W
CC to BB

There normally should be no need to change these jumper positions, however on some units the display may appear too far to the left. If this should occur, change the V to W jumper plug to W to X. This moves the display one character position to the right within the raster.

MODEL III I/O BUS

The Model III Bus was designed to allow easy and convenient interfacing of I/O devices to the Model III. The I/O Bus supports all the signals necessary to implement a device compatible with the Z-80s I/O structure. That is:

Addresses:

A0 to A7 allow selection of up to 256[†] input and 256 output devices if external I/O is enabled.

[†]Ports 80H to 0FFH are reserved for System use.

Data:

DB0 to DB7 allow transfer of 8-bit data onto the processor data bus if external I/O is enabled.

Control Lines:

- IN* — Z-80 signal specifying that an input is in progress. Gated with IORQ.
- OUT* — Z-80 signal specifying that an output is in progress. Gated with IORQ.
- RESET* — system reset signal.
- IOBUSINT* — input to the CPU signaling an interrupt from an I/O Bus device if I/O Bus interrupts are enabled.
- IOBSWAIT* — input to the CPU wait line allowing I/O Bus device to force wait states on the Z-80 if external I/O is enabled.
- EXTIOSEL* — input to CPU which switches the I/O Bus data bus transceiver and allows an INPUT instruction to read I/O Bus data.
- M1* — and IORQ* — standard Z-80 signals

The address line, data line, and control lines a to c and e to g are enabled only when the ENEXIO bit in EC is set to a one.

To enable I/O interrupts, the ENIOBUSINT bit in the CPU IOPORT E0 (output port) must be a one. However, even if it is disabled from generating interrupts, the status of the IOBUSINT* line can still read on the appropriate bit of CPU IOPORT E0 (input port).

See Model III Port Bit assignment for ports 0FF, 0EC, and 0E0 on pages 21 and 22.

The Model III CPU board is fully protected from "foreign I/O devices" in that all the I/O Bus signals are buffered and can be disabled under software control. To attach and use an I/O device on the I/O Bus, certain requirements (both hardware and software) must be met.

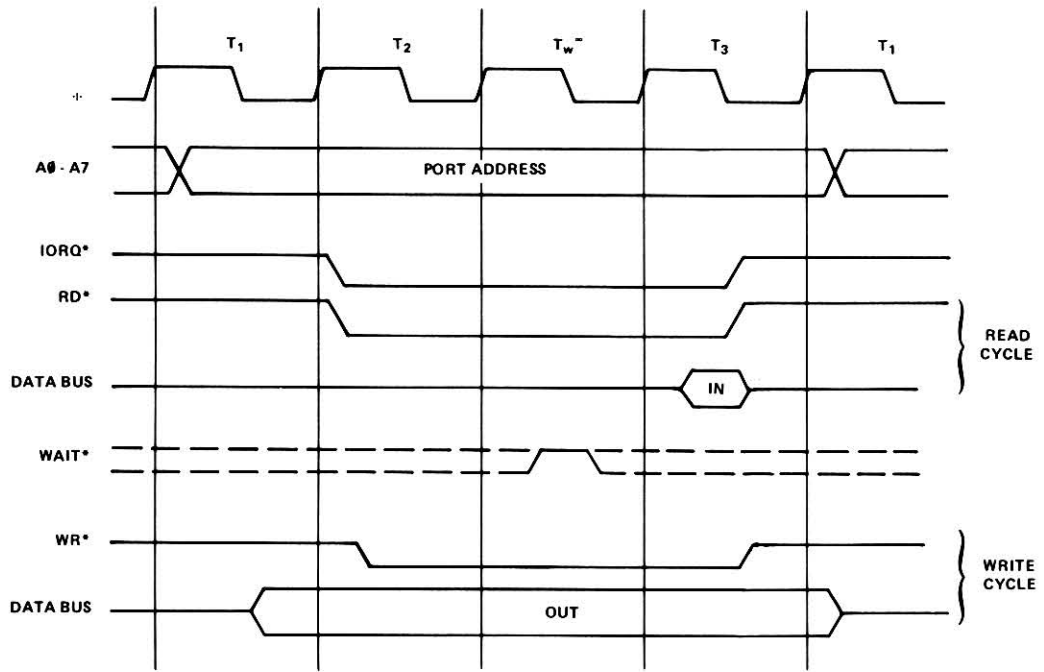
For input port device use, you must enable external I/O devices by writing to port 0ECH with bit 4 on in the user software. This will enable the data bus address lines and control signals to the I/O Bus edge connector. When the input device is selected, the hardware will acknowledge by asserting EXTIOSEL* low. This switches the data bus transceiver and allows the CPU to read the contents of the I/O Bus data lines. See Figure 3 for the timing. EXTIOSEL* can be generated by NANDing IN and the I/O port address.

Output port device use is the same as the input port device in use, in that the external I/O devices must be enabled by writing to port 0ECH with bit 4 on in the user software — in the same fashion.

For either input or output devices, the IOBSWAIT* control line can be used in the normal way for synchronizing slow devices to the CPU. Note that since dynamic memories are used in the Model III, the wait line should be used with caution. Holding the CPU in a wait state for 2 msec or more may cause loss of memory contents since refresh is inhibited during this time. It is recommended that the IOBSWAIT* line be held active no more than 500 μsec with a 25% duty cycle.

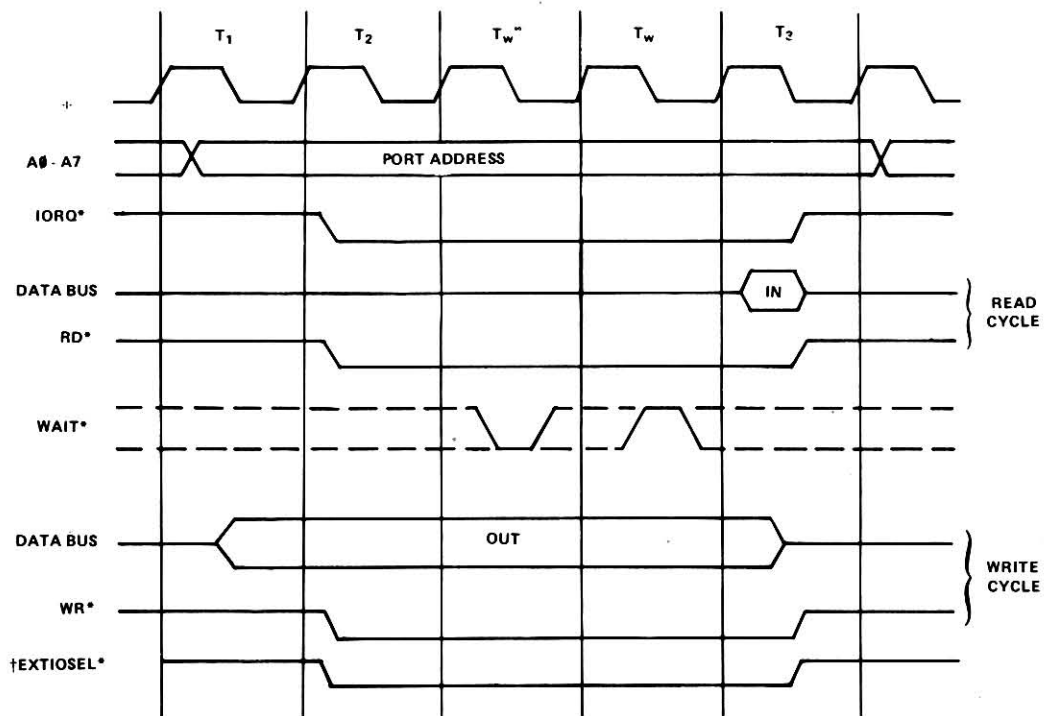
The Model III will support Z-80 mode 1 interrupts. A RAM jump table is supported by the LEVEL II BASIC ROMs and the user must supply the address of his interrupt service routine by writing this address to locations 403E and 403F. When an interrupt occurs, the program will be vectored to the user supplied address if I/O Bus interrupts have been enabled. To enable I/O Bus interrupts, the user must set bit 3 of Port 0E0H.

Input or Output Cycles.



*Inserted by Z80 CPU

Input or Output Cycles with Wait States.



*Inserted by Z80 CPU

†Coincident with IORQ* only on INPUT cycle.

FIGURE 3. I/O BUS TIMING DIAGRAM

MODEL III PORT BITS

Name: WRNMIMASKREG*
Port Address: 0E4H
Access: WRITE ONLY

Bit 7 = ENINTRQ; 0 disables Disk INTRQ from generating an NMI.
1 enables above.

Bit 6 = ENDRQ; 0 disables Disk DRQ from generating an NMI.
1 enables above.

Name: RDNMISTATUS*
Port Address: 0E4H
Access: READ ONLY

Bit 7 = Status of Disk INTRQ; 1 = False, 0 = True

Bit 6 = Status of Disk DRQ; 1 = False, 0 = True

Bit 5 = Reset* Status; 1 = False, 0 = True

Name: MOD OUT
Port Address: 0ECH
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = Undefined

Bit 5 = DISWAIT; 0 disables video waits, 1 enables

Bit 4 = ENEXTIO; 0 disables external IO Bus, 1 enables

Bit 3 = ENALTSET; 0 disables alternate character set,
1 enables alternate video character set.

Bit 2 = MODSEL; 0 enables 64 character mode,
1 enables 32 character mode.

Bit 1 = CASMOTORON; 0 turns cassette motor off,
1 turns cassette motor on.

Bit 0 = Undefined

Name: RDINTSTATUS*
Port Address: 0E0H
Access: READ ONLY

NOTE: A 0 indicates the device is interrupting.

Bit 7 = Undefined

Bit 6 = RS-232 ERROR INT

Bit 5 = RS-232 RCV INT

Bit 4 = RS-232 XMIT INT

Bit 3 = IOBUS INT

Bit 2 = RTC INT

Bit 1 = CASSETTE (1500 Baud) INT F

Bit 0 = CASSETTE (1500 Baud) INT R

Name: CASOUT*
Port Address: 0FFH
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = Undefined

Bit 5 = Undefined

Bit 4 = Undefined

Bit 3 = Undefined

Bit 2 = Undefined

Bit 1 = Cassette output level

Bit 0 = Cassette output level

Name: WRINTMASKREG*
Port Address: 0E0H
Access: WRITE ONLY

Bit 7 = Undefined

Bit 6 = ENERRORINT; 1 enables RS-232 interrupts on parity error, framing error, or data overrun error.
0 disable above.

Bit 5 = ENRCVINT; 1 enables RS-232 receive data register full interrupts,
0 disables above.

Bit 4 = ENXMITINT; 1 enables RS-232 transmitter holding register empty interrupts,
0 disables above.

Bit 3 = ENIOBUSINT; 1 enables I/O Bus interrupts,
0 disables the above.

Bit 2 = ENRTC; 1 enables real time clock interrupt,
0 disables above.

Bit 1 = ENCASINTF; 1 enables 1500 Baud falling edge interrupt,
0 disables above.

Bit 0 = ENCASINTR; 1 enables 1500 Baud rising edge interrupt,
0 disables above.

Name: CAS IN*
Port Address: 0FFH
Access: READ ONLY

Bit 7 = 500 Baud Cassette bit

Bit 6 = Undefined

Bit 5 = DISWAIT (See Port 0E0H definition)

Bit 4 = ENEXTIO (See Port 0E0H definition)

Bit 3 = ENALTSET (See Port 0E0H definition)

Bit 2 = MODSEL (See Port 0E0H definition)

Bit 1 = CASMOTORON (See Port 0E0H definition)

Bit 0 = 1500 Baud Cassette bit

NOTE: Reading Port 0FFH clears the 1500 Baud Cassette interrupts.

Name: DRVSEL*
Port Address: 0F4H
Access: WRITE ONLY

Bit 7 = FM*/MFM; 0 selects single density,
1 selects double density.

Bit 6 = WSGEN; 0 = no wait states generated,
1 = wait states generated.

Bit 5 = PRECOMP; 0 = no write precompensation,
1 = write precompensation enabled.

Bit 4 = SDSEL; 0 selects side 0 of diskette,
1 selects side 1 of diskette.

Bit 3 = Drive select 4

Bit 2 = Drive select 3

Bit 1 = Drive select 2

Bit 0 = Drive select 1

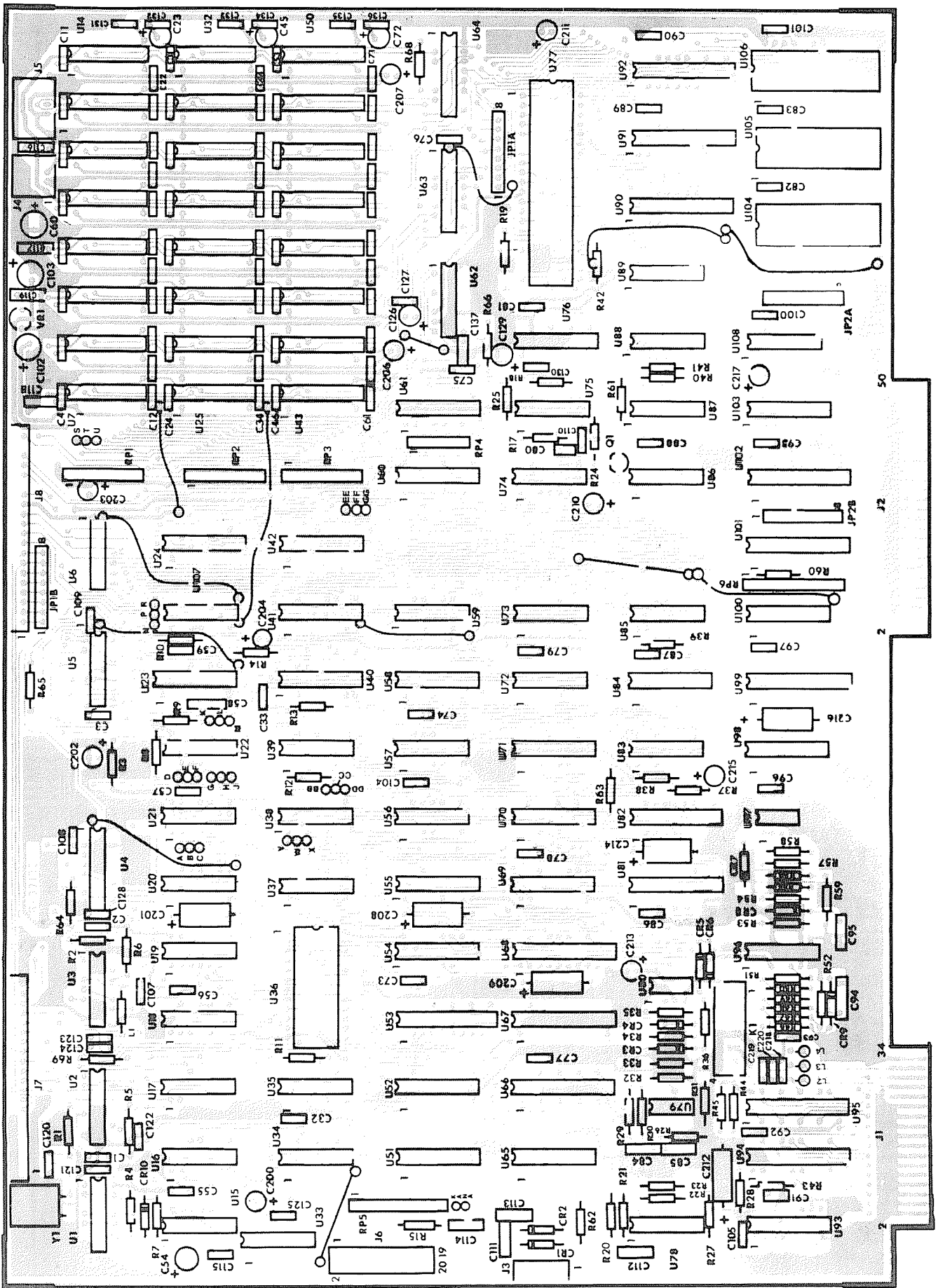


FIGURE 4. CPU PRINTED CIRCUIT BOARD – COMPONENT SIDE

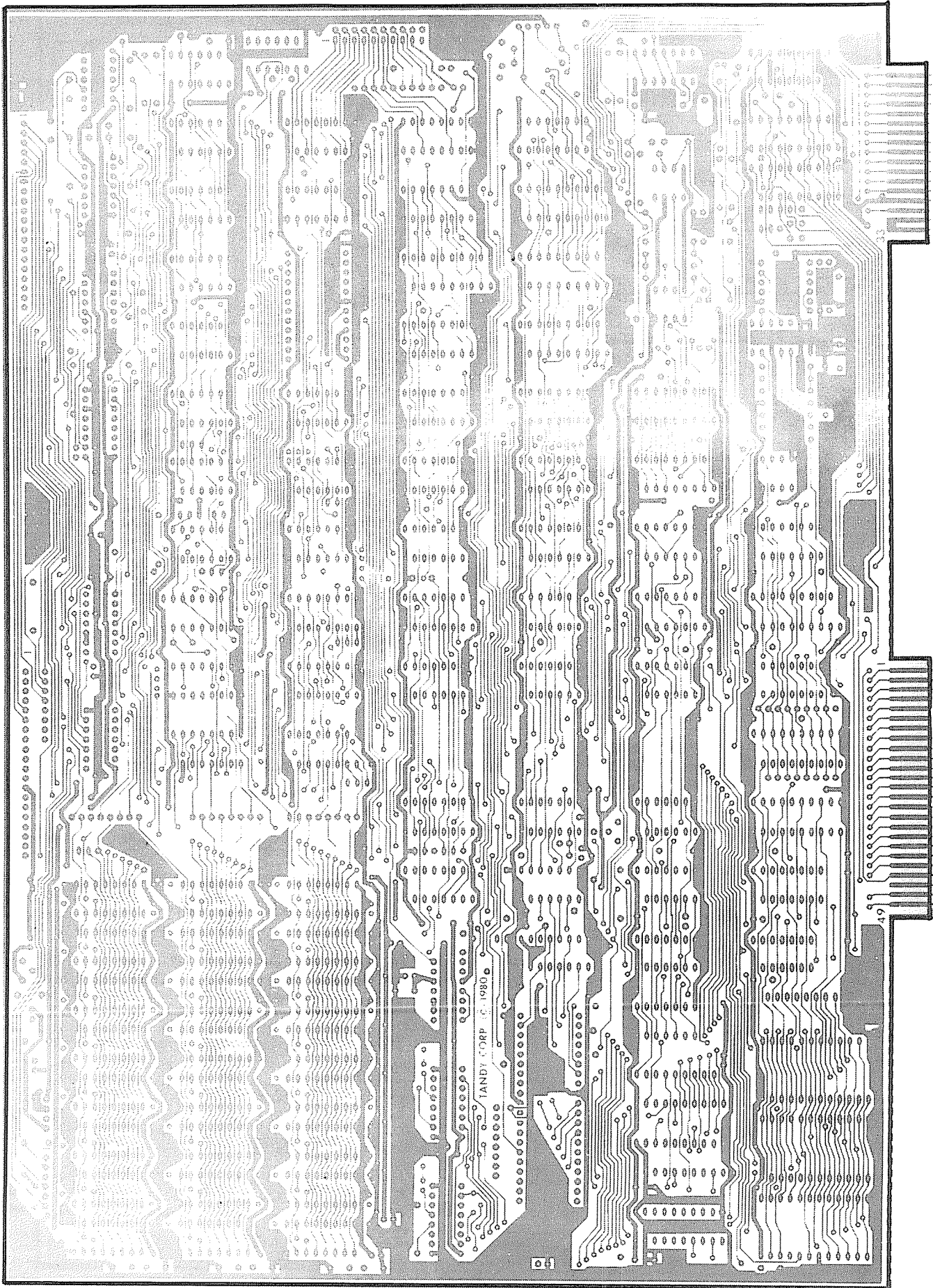


FIGURE 4. CPU PRINTED CIRCUIT BOARD – CIRCUIT SIDE

CPU MODULE PARTS LIST

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|------------|----------------------------------|-------------------------------|----------------------------|
| CAPACITORS | | | |
| C1 | 47pF, Ceramic Disc | 830-0474 | ACC470QJCP |
| C2 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C22 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C23 | 4.7μF, 16V, Electrolytic, Radial | 832-5471 | ACC4752DAP |
| C24 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C44 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C45 | 4.7μF, 16V, Electrolytic, Radial | 832-5471 | ----- |
| C46 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C53 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C54 | 22μF, 16V, Electrolytic, Radial | 832-6221 | ----- |
| C55 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C56 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C57 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C58 | 4700pF, Ceramic Disc | 830-2473 | ----- |
| C59 | 0.0047μF, Ceramic Disc | ----- | ----- |
| C60 | 33μF, | 832-6331 | ACC336QDAP |
| C61 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C71 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C72 | 4.7μF, 16V, Electrolytic, Radial | 832-5471 | ACC4752DAP |
| C73 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C79 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C80 | 33pF, Ceramic Disc | 830-0334 | ACC330QJCP |
| C81 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C82 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C83 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C84 | 0.001μF, Ceramic Disc | 830-2104 | ACC102QJCP |
| C85 | 0.001μF, Ceramic Disc | 830-2104 | ACC102QJCP |
| C86 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C90 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C91 | 200pF, Ceramic Disc | 830-1204 | ACC201QJCP |
| C92 | 0.1μF, 50V, Monolithic | 838-4104 | ACC104QJAP |
| C93 | 4700pF, Ceramic Disc | 830-2474 | ----- |
| C94 | 0.1μF, Ceramic Disc | 830-4104 | ACC104QJAP |
| C95 | 0.01μF, Ceramic Disc | 830-3104 | ACC103QJCP |

CPU MODULE PARTS LIST (cont'd)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|--------|---------------------------------------|-------------------------------|----------------------------|
| C96 | 0.1 μ F, 50V, Monolithic | 830-4104 | ACC104QJAP |
| ↓ | ↓ | ↓ | ↓ |
| C101 | 0.1 μ F, 50V, Monolithic | 830-4104 | ACC104QJAP |
| C102 | 10 μ F, Electrolytic, Radial | 832-6101 | ACC106QDAP |
| C103 | 10 μ F, Electrolytic, Radial | 832-6101 | ACC106QDAP |
| C104 | 0.1 μ F, 50V, Monolithic | 830-4104 | ACC104QJAP |
| C105 | 0.1 μ F, 50V, Monolithic | 830-4104 | ACC104QJAP |
| C106 | 0.01 μ F, Ceramic Disc | 830-3104 | ACC103QJCP |
| C107 | 27pF, Ceramic Disc | 830-0274 | ----- |
| C108 | 220pF, 50V, Z5P, Ceramic Disc | 830-1223 | ACC101QJCP |
| C109 | 100pF, 50V, Ceramic Disc | 830-1104 | ACC101QJCP |
| C110 | 100pF, 50V, Ceramic Disc | 830-1104 | ACC101QJCP |
| C111 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| ↓ | ↓ | ↓ | ↓ |
| C115 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C116 | 100pF, 50V, Ceramic Disc | 830-1104 | ACC101QJCP |
| C117 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C118 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C119 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C120 | 180pF, Ceramic Disc | 830-1184 | ----- |
| C121 | 220pF, Ceramic Disc | 830-1223 | ----- |
| C122 | 27pF, Ceramic Disc | 830-0274 | ACC470QJCP |
| C123 | 220pF, Ceramic Disc | 830-1223 | ----- |
| C124 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C125 | 100pF, 50V, Ceramic Disc | 830-1104 | ----- |
| C126 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C127 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C128 | 100pF, 50V, Ceramic Disc | 830-1104 | ACC0130QJCP |
| C129 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C130 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| ↓ | ↓ | ↓ | ↓ |
| C136 | 0.022 μ F, Ceramic Disc | 830-3224 | ----- |
| C137 | 220pF, Ceramic Disc | 830-1223 | ----- |
| C138 | Not Used | ----- | ----- |
| ↓ | ↓ | ↓ | ↓ |
| C199 | Not Used | ----- | ----- |
| C200 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C201 | 10 μ F, 16V, Electrolytic, axial | 831-6101 | ----- |
| C202 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| ↓ | ↓ | ↓ | ↓ |
| C207 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C208 | 10 μ F, 16V, Electrolytic, axial | 831-6101 | ----- |
| C209 | 10 μ F, 16V, Electrolytic, axial | 831-6101 | ----- |
| C210 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C211 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C212 | 10 μ F, 16V, Electrolytic, axial | 831-6101 | ----- |
| C213 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C214 | 10 μ F, 16V, Electrolytic, axial | 831-6101 | ----- |
| C215 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |
| C216 | 10 μ F, 16V, Electrolytic, axial | 831-6101 | ----- |
| C217 | 10 μ F, 16V, Electrolytic, radial | 832-6101 | ACC106QDAP |

CPU MODULE PARTS LIST (cont'd)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|--------|--------------------|----------------------------|-------------------------|
| C218 | 68pF, Ceramic Disc | 830-0684 | ACC680QJCP |
| C219 | 68pF, Ceramic Disc | 830-0684 | ACC680QJCP |
| C220 | 68pF, Ceramic Disc | 830-0684 | ACC680QJCP |

CONNECTORS

| | | | |
|------|---------------------------------|----------|--------|
| J3 | Right Angle Header Connector | 851-9091 | AJ6978 |
| J4 | 4-pin Header Connector | 851-9079 | AJ6997 |
| J5 | 6-pin Header Connector | 851-9103 | AJ6980 |
| J6 | 20 position | 851-9086 | AJ6848 |
| J7 | 20 position, straight connector | 851-9101 | AJ6979 |
| J8 | 20 position, straight connector | 851-9101 | AJ6979 |
| JP1A | DIP Strip, 8-position | 851-9105 | AJ6981 |
| JP1B | DIP Strip, 8-position | 851-9105 | AJ6981 |
| JP2A | DIP Strip, 8-position | 851-9105 | AJ6981 |
| JP2B | DIP Strip, 8-position | 851-9105 | AJ6981 |

CRYSTAL

| | | | |
|----|-------------|----------|-------|
| Y1 | 10.1376 MHz | 840-9007 | ----- |
|----|-------------|----------|-------|

DIODES

| | | | |
|-----|--------|----------|----------|
| CR1 | 1N982 | 815-0982 | ADX1103 |
| CR2 | 1N982 | 815-0982 | ADX-1103 |
| CR3 | 1N4148 | 815-0148 | ADX-1152 |
| ↓ | ↓ | ↓ | ↓ |
| CR9 | 1N4148 | 815-0148 | ADX-1152 |

FERRITE BEADS

| | | | |
|-----|-------------|----------|-------|
| L1 | #2643000301 | 841-9014 | ----- |
| FB1 | #2673000701 | 841-9019 | ----- |
| FB2 | #2673000701 | 841-9019 | ----- |
| FB3 | #2673000701 | 841-9019 | ----- |

INTEGRATED CIRCUITS

| | | | |
|-----|------------------------------------|----------|---------|
| U1 | 74LS74, Dual "D" Flip-Flop | 802-0074 | AMX3558 |
| U2 | 74LS04, Hex Inverter | 802-0004 | AMX3552 |
| U3 | 74LS74, Dual "D" Flip-Flop | 802-0074 | AMX3558 |
| U4 | 74LS157, Quad 1-of-2 Data Selector | 802-0157 | AMX3563 |
| U5 | 74LS93, Binary (÷16) Counter | 802-0093 | AMX3560 |
| U6 | 74LS10, Tripe 3-input NAND gate | 802-0010 | AMX3898 |
| U7 | 416, RAM | 804-1016 | AXX3021 |
| ↓ | ↓ | ↓ | ↓ |
| U14 | 416, RAM | 804-1016 | AXX3021 |
| U15 | 74LS132, Quad 2-input NAND | 802-0132 | AMX3561 |
| U16 | 74LS00, Quad 2-input NAND gate | 802-0000 | AMX3550 |
| U17 | 74LS74, Dual "D" Flip-Flop | 802-0074 | AMX3558 |

CPU-MODULE PARTS LIST (cont'd)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|--------|---|-------------------------------|----------------------------|
| U18 | 74LS00, Quad 2-input NAND gate | 802-0000 | AMX3550 |
| U19 | 74LS08, Quad 2-input AND gate | 802-0008 | AMX3698 |
| U20 | 74LS393, | 802-0393 | AMX3706 |
| U21 | 74LS11, Triple 3-input AND gate | 802-0011 | AMX3554 |
| U22 | 74LS246, | 802-0266 | ----- |
| U23 | 74LS221, Dual One-Shot with Schmitt Trigger input | 802-0221 | AMX3810 |
| U24 | 74157, Quad 2-Line to 1-Line Data Selector/Multiplexer | 802-0157 | AMX3563 |
| U25 | 416, RAM | 804-1016 | AXX3021 |
| ↓ | ↓ | ↓ | ↓ |
| U32 | 416, RAM | 804-1016 | AXX3021 |
| U33 | 74LS04, Hex Inverter | 802-0004 | AMX3552 |
| U34 | 74LS05, Hex Inverter with Open Collector | 802-0005 | AMX3553 |
| U35 | 74LS05, Hex Inverter with Open Collector | 802-0005 | AMX3553 |
| U36 | MCM68A316E, Character Generator | 804-4316 | AXX3040 |
| U37 | 74LS00, Quad 2-input NAND gate | 802-0000 | AMX3550 |
| U38 | 74LS266, Quad Exclusive NOR gate with Open Collector Outputs | 802-0266 | AMX4660 |
| U39 | 74LS08, Quad 2-input AND gate | 802-0008 | AMX3698 |
| U40 | 74LS138, Decoder/De-multiplexer | 802-0138 | AMX4583 |
| U41 | 74LS138, Decoder/De-multiplexer | 802-0138 | AMX4583 |
| U42 | 74157, Quad 2-Line to 1-Line Data Selector/Multiplexer | 802-0157 | AMX3563 |
| U43 | 416, RAM | 804-1016 | AXX3021 |
| ↓ | ↓ | ↓ | ↓ |
| U50 | 416, RAM | 804-1016 | AXX3021 |
| U51 | MC14050B | 803-0050 | AMX4584 |
| U52 | 74LS166, 8-bit Parallel In/Serial Out Shift Register | 802-0166 | AMX3564 |
| U53 | 74LS244, Line Driver | 802-0244 | AMX3864 |
| U54 | 74LS153, Dual 4-line to 1-line Data Selector/Multiplexer | 802-1053 | AMX3562 |
| U55 | 74LS175, Hex/Quad "D" Flip-Flop with Clear | 802-0175 | AMX3566 |
| U56 | 74LS393 | 802-0393 | AMX3706 |
| U57 | 74LS02, Quad 2-input NOR gate | 802-0002 | AMX3551 |
| U58 | 74LS139, Decoder/De-multiplexer | 802-0139 | AMX3800 |
| U59 | 74LS32, Quad 2-input OR gate | 802-0032 | AMX3557 |
| U60 | 74LS145, BCD/Decimal Decoder/Driver | 802-0145 | AMX4659 |
| U61 | 74LS175, Hex/Quad "D" Flip-Flop | 802-0175 | AMX3566 |
| U62 | 74LS90, Decade, (÷12), Binary Counter | 802-0090 | AMX3804 |
| U63 | 8T26, Bus Transceiver | 806-0026 | AMX4261 |
| U64 | 8T26, Bus Transceiver | 806-0026 | AMX4261 |

CPU MODULE PARTS LIST (cont'd)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|--------|---|-------------------------------|----------------------------|
| U65 | MC14050B | 803-0050 | AMX4584 |
| U66 | 74LS240, Octal Buffer | 802-0240 | AMX4225 |
| U67 | 74LS245 | 802-0245 | AMX4470 |
| U68 | 74LS273 | 802-0273 | AMX4227 |
| U69 | 74LS157, Quad 2-line to 1-line Data Selector/Multiplexer | 802-0157 | AMX3563 |
| U70 | 74LS157, Quad 2-line to 1-line Data Selector/Multiplexer | 802-0157 | AMX3563 |
| U71 | 74LS157, Quad 2-line to 1-line Data Selector/Multiplexer | 801-0157 | AMX3563 |
| U72 | 74LS30, 8-input NAND gate | 802-0030 | AMX3556 |
| U73 | 74LS27, Triple 3-input NOR gate | 802-0027 | AMX4658 |
| U74 | 74LS04, Hex Inverter Quad 2-input | 802-0004 | AMX3552 |
| U75 | 74LS08, Quad 2-input AND gate | 802-0008 | AMX3698 |
| U76 | 74LS367, Tri-State Hex Buffer | 802-0367 | AMX3567 |
| U77 | Z-80, CPU | 804-7080 | AMX3586 |
| U78 | 74LS74, Dual "D" Flip-Flop Positive Edge Triggered | 802-0074 | AMX3558 |
| U79 | MC1741, Operational Amplifier | 805-0741 | AMX4258 |
| U80 | MC1458 | 805-0458 | AMX4661 |
| U81 | MCM2114, RAM | 804-0004 | AXX3038 |
| U82 | MCM2114, RAM | 804-0004 | AXX3038 |
| U83 | 74LS74, Dual "D" Flip-Flop Positive Edge Triggered | 802-0074 | AMX3558 |
| U84 | 74LS367, Tri-State Hex Buffer | 802-0367 | AMX3567 |
| U85 | 74LS74, Dual "D" Flip-Flop Positive Edge Triggered | 802-0074 | AMX3558 |
| U86 | 74LS32, Quad 2-input OR gate | 802-0032 | AMX3557 |
| U87 | 74LS04, Hex Inverter | 802-0004 | AMX3552 |
| U88 | 74LS38, Quad 2-input NAND Buffer with Open Collector Outputs | 802-0038 | AMX4328 |
| U89 | 74LS32, Quad 2-input OR gate | 802-0032 | AMX3557 |
| U90 | 74LS245 | 802-0245 | AMX4470 |
| U91 | 74LS244, Line Driver | 802-0244 | AMX3864 |
| U92 | 74LS244, Line Driver | 802-0244 | AMX3864 |
| U93 | Not Used | ----- | ----- |
| U94 | 74LS273, Octal "D" Flip-Flop | 802-0273 | AMX4227 |
| U95 | 74LS244, Line Driver | 802-0244 | AMX3864 |
| U96 | LM339 | 805-0339 | AMX4200 |
| U97 | MC75452 | 805-0452 | AMX3573 |
| U98 | 74LS174, Hex Quad "D" Flip-Flop | 802-0174 | AMX3565 |
| U99 | 74LS244, Line Driver | 802-0244 | AMX3864 |
| U100 | 74LS174, Hex Quad "D" Flip-Flop | 802-0174 | AMX3565 |
| U101 | 74LS245 | 802-0245 | AMX4470 |
| U102 | 74LS244, Line Driver | 802-0244 | AMX3864 |
| U103 | 74LS367, Tri-State Hex Buffer | 802-0367 | AMX3567 |
| U104 | ROM A, MCM364 | 804-1364 | AXX3039 |
| U105 | ROM B, MCM332 | 804-0332 | AXX3037 |
| U106 | ROM C, MCM68A | 804-0316B | AMX4642 |
| U107 | 74LS32, Quad 2-input OR gate | 802-0032 | AMX3557 |
| U108 | 74LS10, Triple 3-input NAND gate | 802-0010 | AMX3898 |

CPU MODULE PARTS LIST (cont'd)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|-----------|------------------------------|-------------------------------|----------------------------|
| RESISTORS | | | |
| R1* | 910 ohm, ¼W, 5%, Carbon Film | 820-7191 | AN0192EEC |
| R2 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R3 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R4 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R5* | 910 ohm, ¼W, 5%, Carbon Film | 820-7191 | AN0192EEC |
| R6 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R7 | 100K, ¼W, 5%, Carbon Film | 820-7410 | AN0371EEC |
| R8 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R9 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R10 | 2.7K, ¼W, 5%, Carbon Film | 820-7227 | AN0224EEC |
| R11 | 470 ohm, ¼W, 5%, Carbon Film | ----- | ----- |
| R12 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R13 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R14 | 10K, ¼W, 5%, Carbon Film | 820-7310 | AN0281EEC |
| R15 | 750 ohm, ¼W, 5%, Carbon Film | 820-7175 | ----- |
| R16 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R17 | 1.2K, ¼W, 5%, Carbon Film | 820-7212 | AN0199EEC |
| R18 | 22 ohm, ¼W, 5%, Carbon Film | 820-7022 | AN0078EEC |
| R19 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R20 | 220K, ¼W, 5%, Carbon Film | 820-7422 | AN0396EEC |
| R21 | 7.5K, ¼W, 5%, Carbon Film | 820-7275 | ----- |
| R22 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R23 | 7.5K, ¼W 5%, Carbon Film | 820-7275 | ----- |
| R24 | 220 ohm, ¼W, 5%, Carbon Film | 820-7122 | AN0149EEC |
| R25 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R26 | 82K, ¼W, 5%, Carbon Film | 820-7382 | ----- |
| R27 | 1.2K, ¼W, 5%, Carbon Film | 820-7212 | AN0199EEC |
| R28 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R29 | 75K, ¼W, 5%, Carbon Film | 820-7375 | ----- |
| R30 | 39K, ¼W, 5%, Carbon Film | 820-7339 | AN0330EEC |
| R31 | 100K, ¼W, 5%, Carbon Film | 820-7410 | AN0371EEC |
| R32 | 220 ohm, ¼W, 5%, Carbon Film | 820-7122 | AN0149EEC |
| R33 | 100K, ¼W, 5%, Carbon Film | 820-7410 | AN0371EEC |
| R34 | 100K, ¼W, 5%, Carbon Film | 820-7410 | AN0371EEC |
| R35 | 100K, ¼W, 5%, Carbon Film | 820-7410 | AN0371EEC |
| R36 | 100K, ¼W, 5%, Carbon Film | 820-7410 | AN0371EEC |
| R37 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R38 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R39 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R40 | 150 ohm, ¼W, 5%, Carbon Film | 820-7115 | AN0142EEC |
| R41 | 150 ohm, ¼W, 5%, Carbon Film | 820-7115 | AN0142EEC |
| R42 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R43 | 20K, ¼W, 5%, Carbon Film | 820-7320 | ----- |
| R44 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R45 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R46 | 10K, ¼W, 5%, Carbon Film | 820-7310 | AN0281EEC |
| R47 | 10K, ¼W, 5%, Carbon Film | 820-7310 | AN0281EEC |
| R48 | 51K, ¼w, 5%, Carbon Film | 820-7351 | ANO344EEC |
| R49 | 10K, ¼W, 5%, Carbon Film | 820-7310 | AN0281EEC |

* May appear as 560 ohm

820-7156

CPU MODULE PARTS LIST (cont'd)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------|------------------------------|-------------------------------|----------------------------|
| R50 | 4.7K, ¼W, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R51 | 620K, ¼W, 5%, Carbon Film | 820-7462 | ----- |
| R52 | 10K, ¼W, 5%, Carbon Film | 820-7310 | AN0281EEC |
| R53 | 8.2K, ¼W, 5%, Carbon Film | 820-7282 | AN0271EEC |
| R54 | 6.8K, ¼W, 5%, Carbon Film | 820-7268 | ----- |
| R55 | 56K, ¼W, 5%, Carbon Film | 820-7356 | ----- |
| R56 | 56K, ¼W, 5%, Carbon Film | 820-7356 | ----- |
| R57 | 1.5M, ¼W, 5%, Carbon Film | 820-7515 | ----- |
| R58 | 1K, ¼w, 5%, Carbon Film | 820-7210 | AN0196EEC |
| R59 | 15K, ¼W, 5%, Carbon Film | 820-7315 | AN0297EEC |
| R60 | 150 ohm, ¼w, 5%, Carbon Film | 820-7115 | AN0142EEC |
| R61 | 10K, ¼W, 5%, Carbon Film | 820-7310 | AN0281EEC |
| R62 | 220 ohm, ¼w, 5%, Carbon Film | 820-7122 | AN0149EEC |
| R63 | 4.7K, ¼w, 5%, Carbon Film | 820-7247 | AN0247EEC |
| R64 | 22K, ¼W, 5%, Carbon Film | 820-7322 | ----- |
| R65 | 47 ohm, ¼W, 5%, Carbon Film | 820-7047 | AN0099EEC |
| R66 | 30 ohm, ¼W, 5%, Carbon Film | 820-7030 | ----- |
| R67 | Not Used | ----- | ----- |
| R68 | Not Used | ----- | ----- |
| R69 | 220 ohm, ¼W, 5%, Carbon Film | 820-7122 | ----- |
| RP1 | 27 ohm, Resistor Network | 829-0009 | ----- |
| RP2 | 27 ohm, Resistor Network | 829-0009 | ----- |
| RP3 | 27 ohm, Resistor Network | 829-0009 | ----- |
| RP4 | 4.7K, Resistor Network | 829-3247 | ----- |
| RP5 | 1.5K, Resistor Network | 829-0015 | ----- |
| RP6 | 10K, Resistor Network | 829-0010 | ----- |
| RELAY | | | |
| K1 | 1 Form A, 5VDC | 842-9102 | AR8130 |
| TRANSISTORS | | | |
| Q1 | 2N3906 | 810-0906 | AMX3584 |
| VR1 | MC7905C | 805-1905 | AMX4260 |
| MISCELLANEOUS | | | |
| | Cable, 8-position, 3.75" (1) | 845-9008 | ----- |
| | Cable, 8-position, 8.5" (1) | 845-9108 | AW2632 |
| | Jumper Plugs (10) | 851-9098 | ----- |
| | Socket, 40-pin (1) | 850-9002 | AJ6580 |
| | Socket, 24-pin (4) | 850-9001 | AJ6579 |
| | Socket, 20-pin (3) | 850-9009 | AJ6760 |
| | Socket, 18-pin (2) | 850-9006 | AJ6701 |
| | Socket, 16-pin (24) | 850-9003 | AJ6581 |

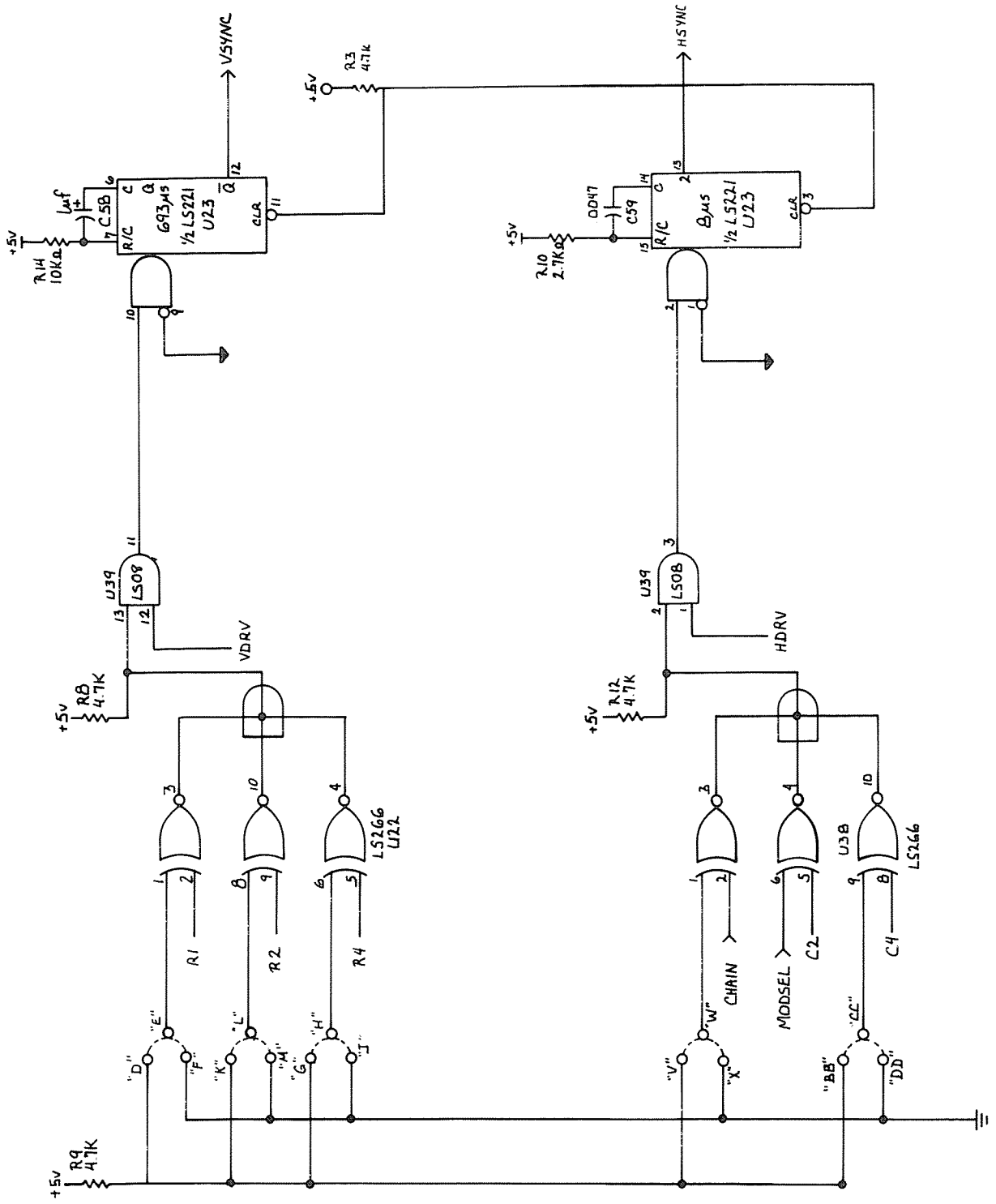
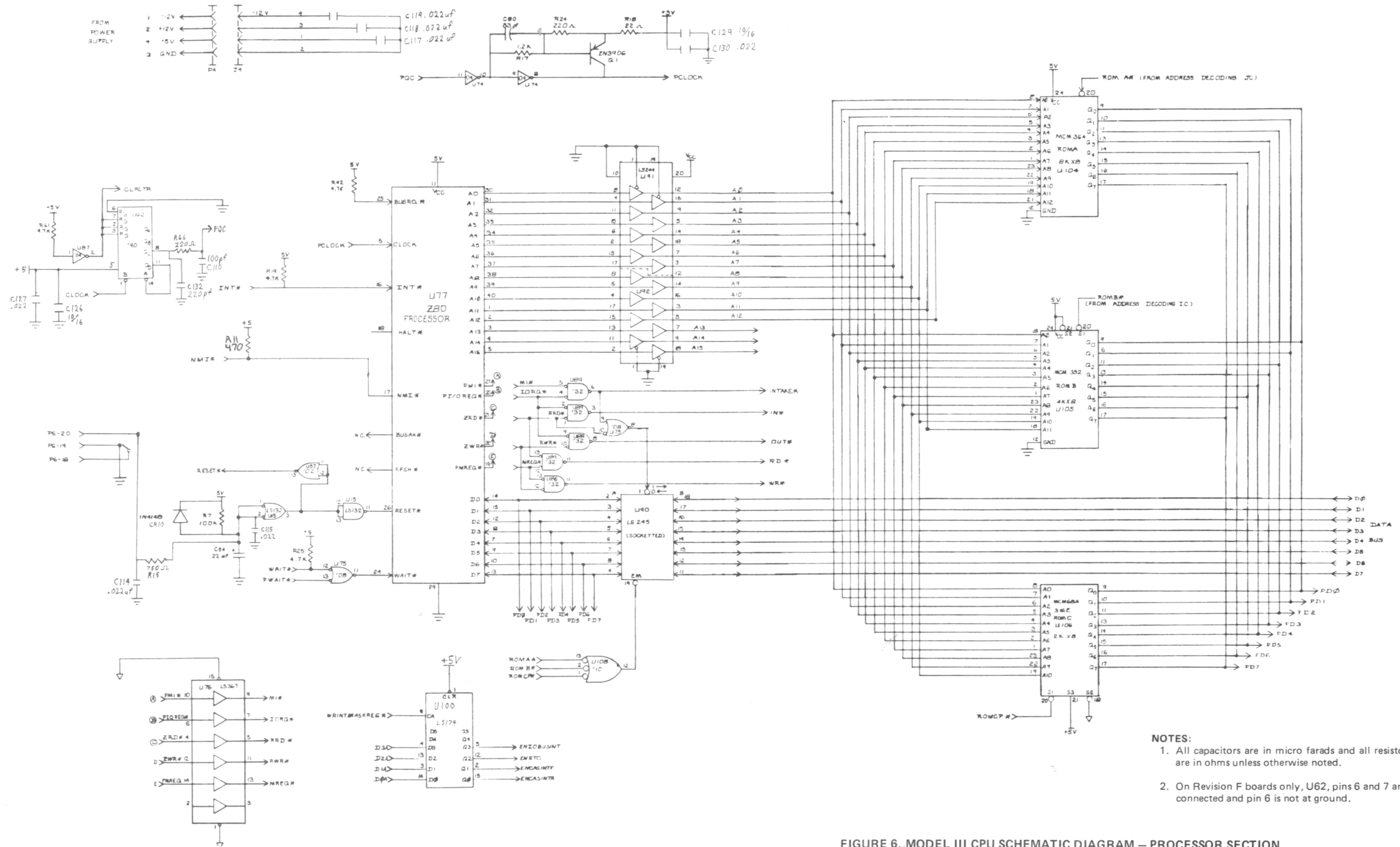


FIGURE 5. MODEL III CPU SCHEMATIC DIAGRAM – VIDEO AND HORIZONTAL SYNC. CIRCUITS



NOTES:

1. All capacitors are in micro farads and all resistors are in ohms unless otherwise noted.
2. On Revision F boards only, U62, pins 6 and 7 are connected and pin 6 is not at ground.

FIGURE 6. MODEL III CPU SCHEMATIC DIAGRAM – PROCESSOR SECTION

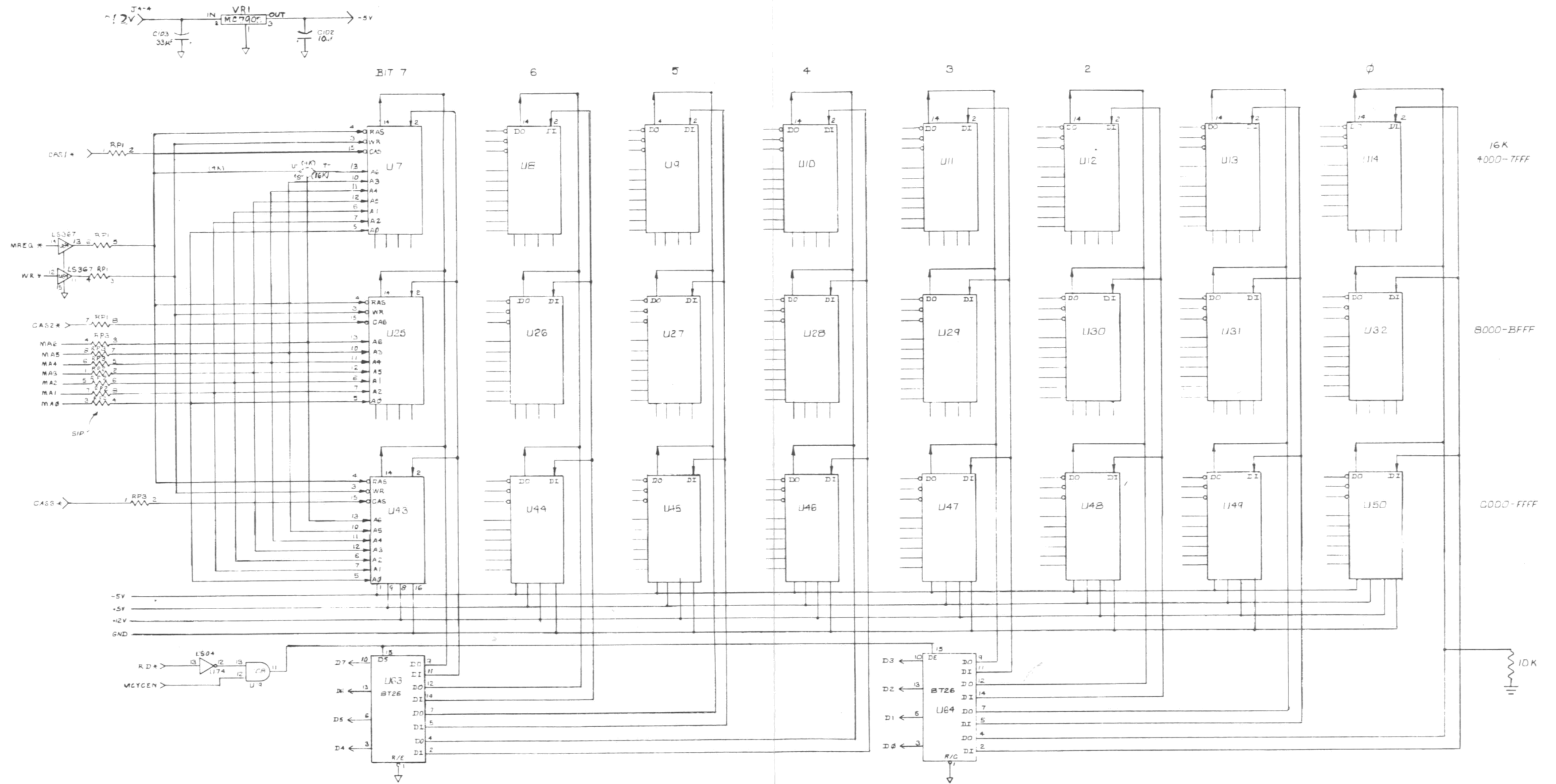


FIGURE 7. MODEL III CPU SCHEMATIC DIAGRAM – RAM SECTION

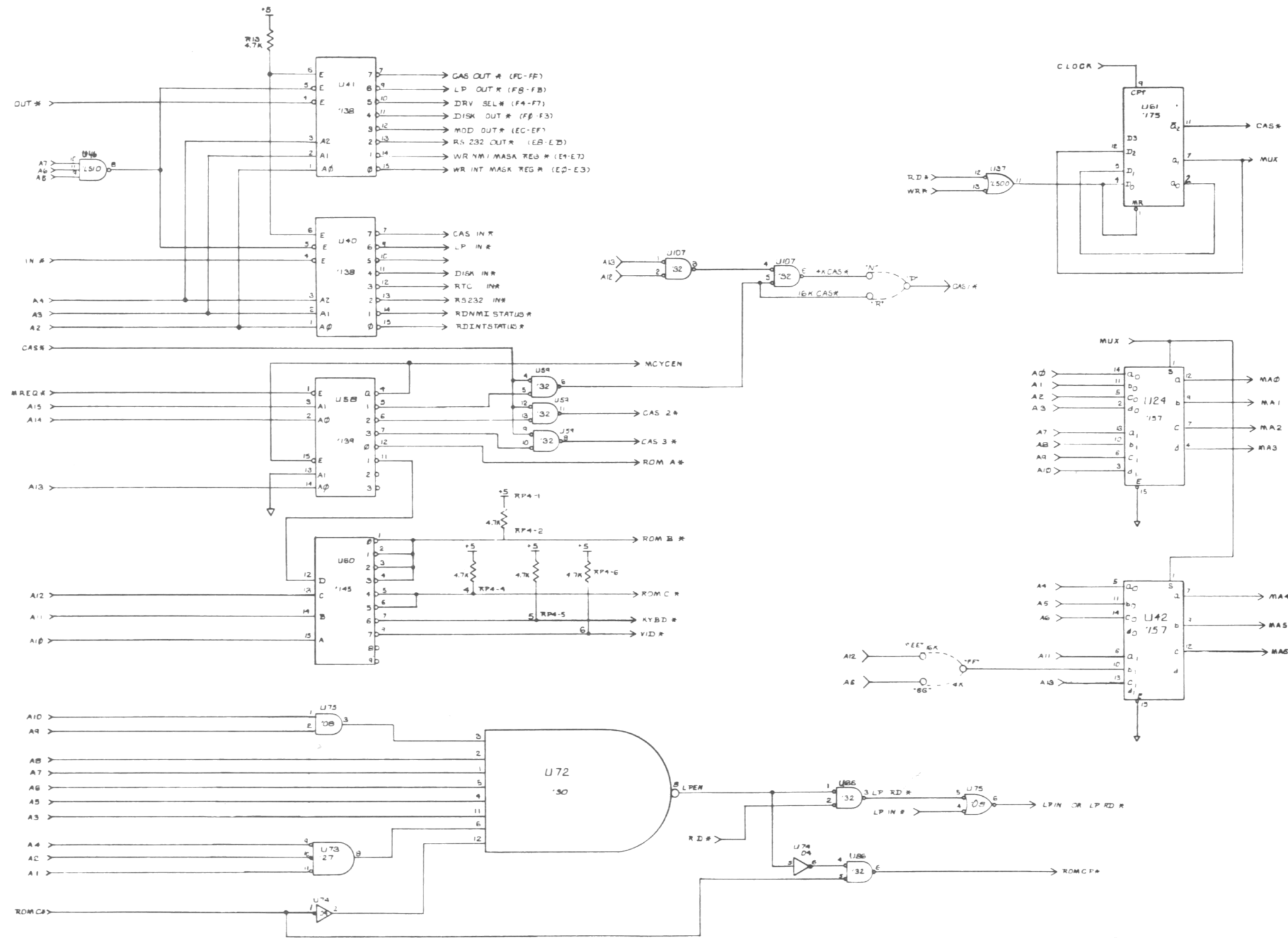


FIGURE 8. MODEL III CPU SCHEMATIC DIAGRAM – ADDRESS DECODING SECTION

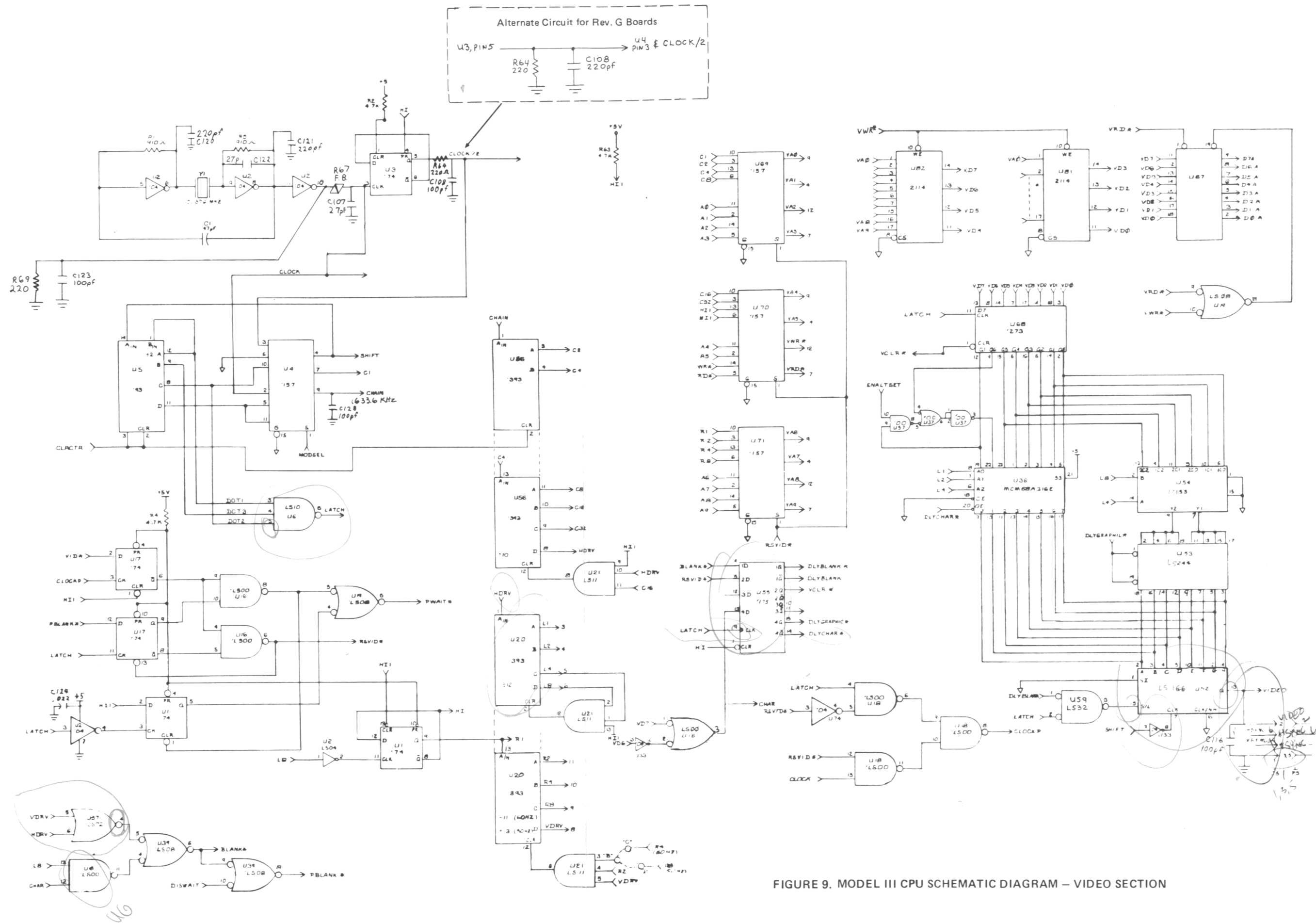
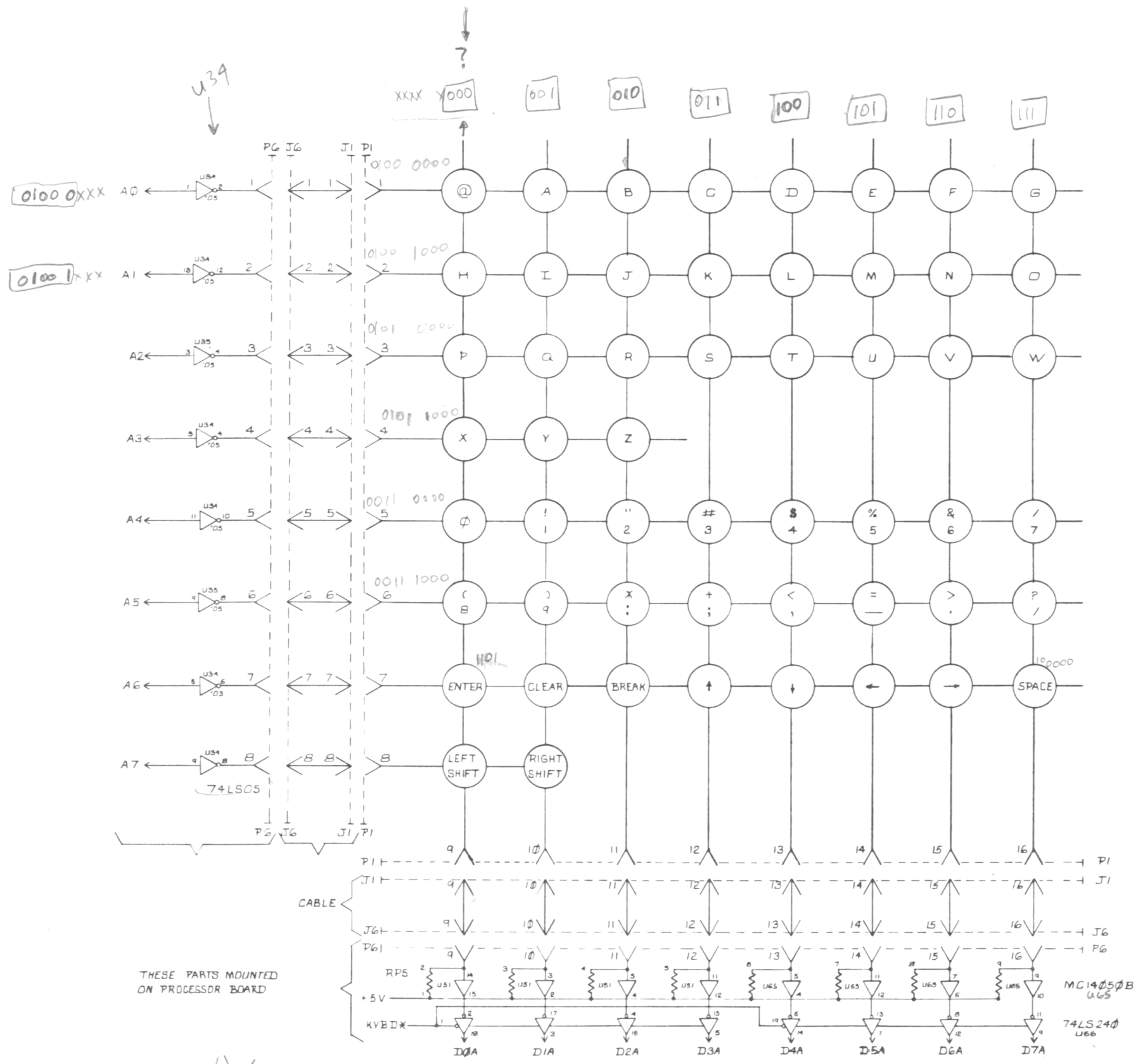
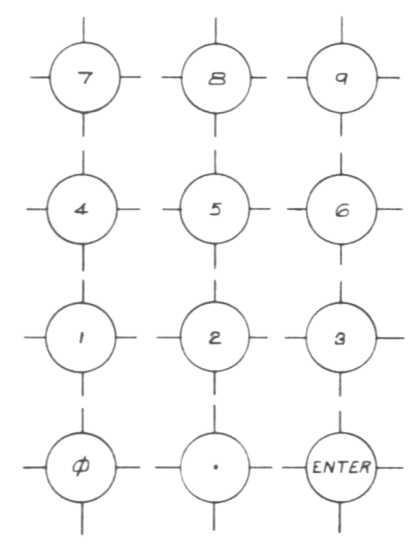
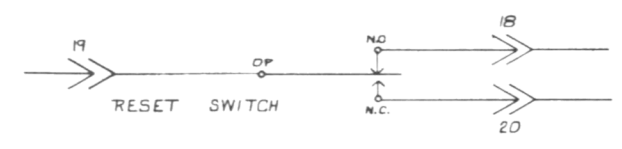


FIGURE 9. MODEL III CPU SCHEMATIC DIAGRAM – VIDEO SECTION



THESE PARTS MOUNTED ON PROCESSOR BOARD

U51
U65



THE ABOVE KEYS (MODES) ARE CONNECTED IN PARALLEL WITH THE SIMILAR KEYS OF THE KEYBOARD MATRIX.

RP5 = 3250 Ω

FIGURE 10. MODEL III CPU SCHEMATIC DIAGRAM – KEYBOARD SECTION

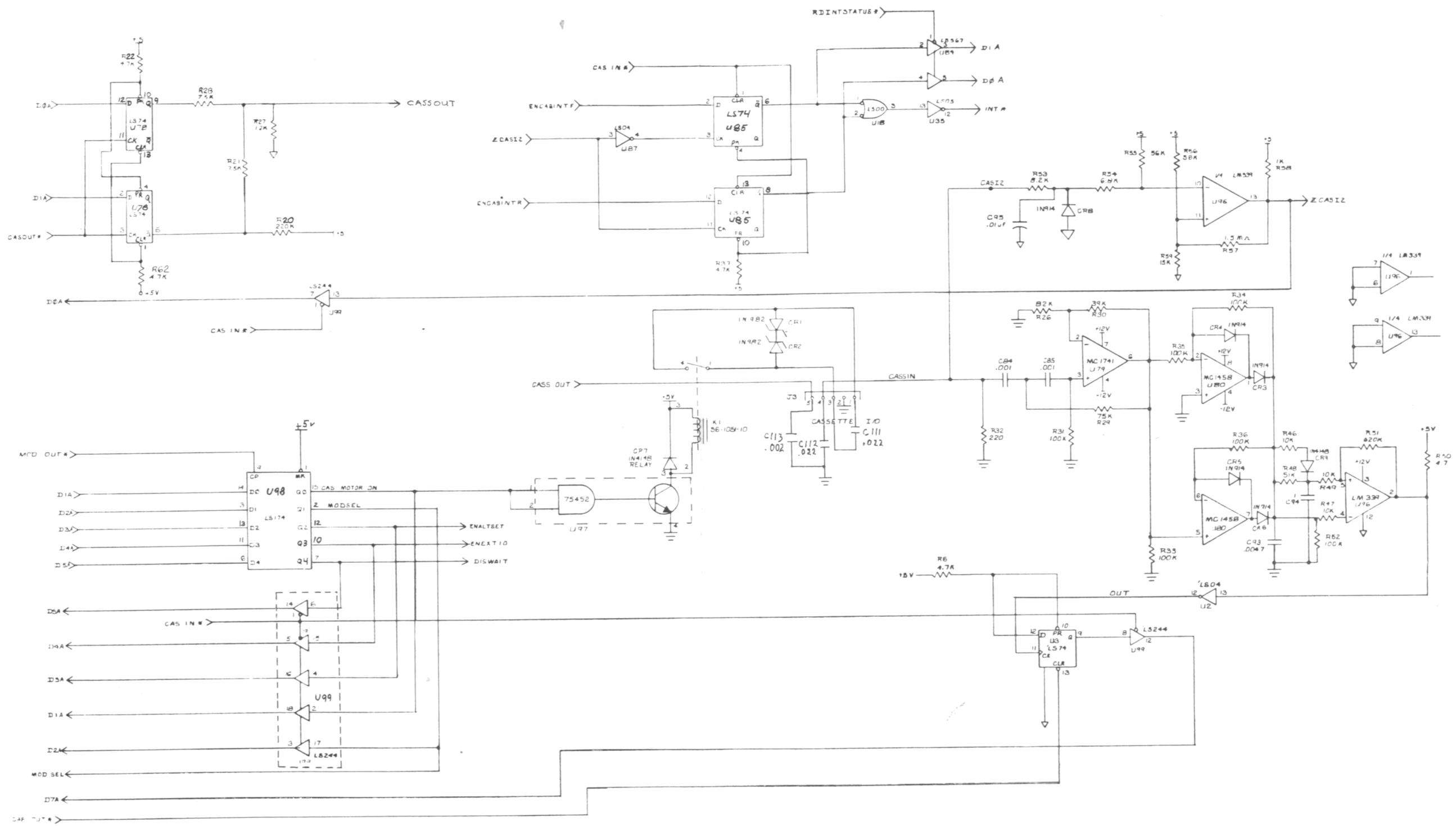


FIGURE 11. MODEL III CPU SCHEMATIC DIAGRAM – CASSETTE INTERFACE SECTION

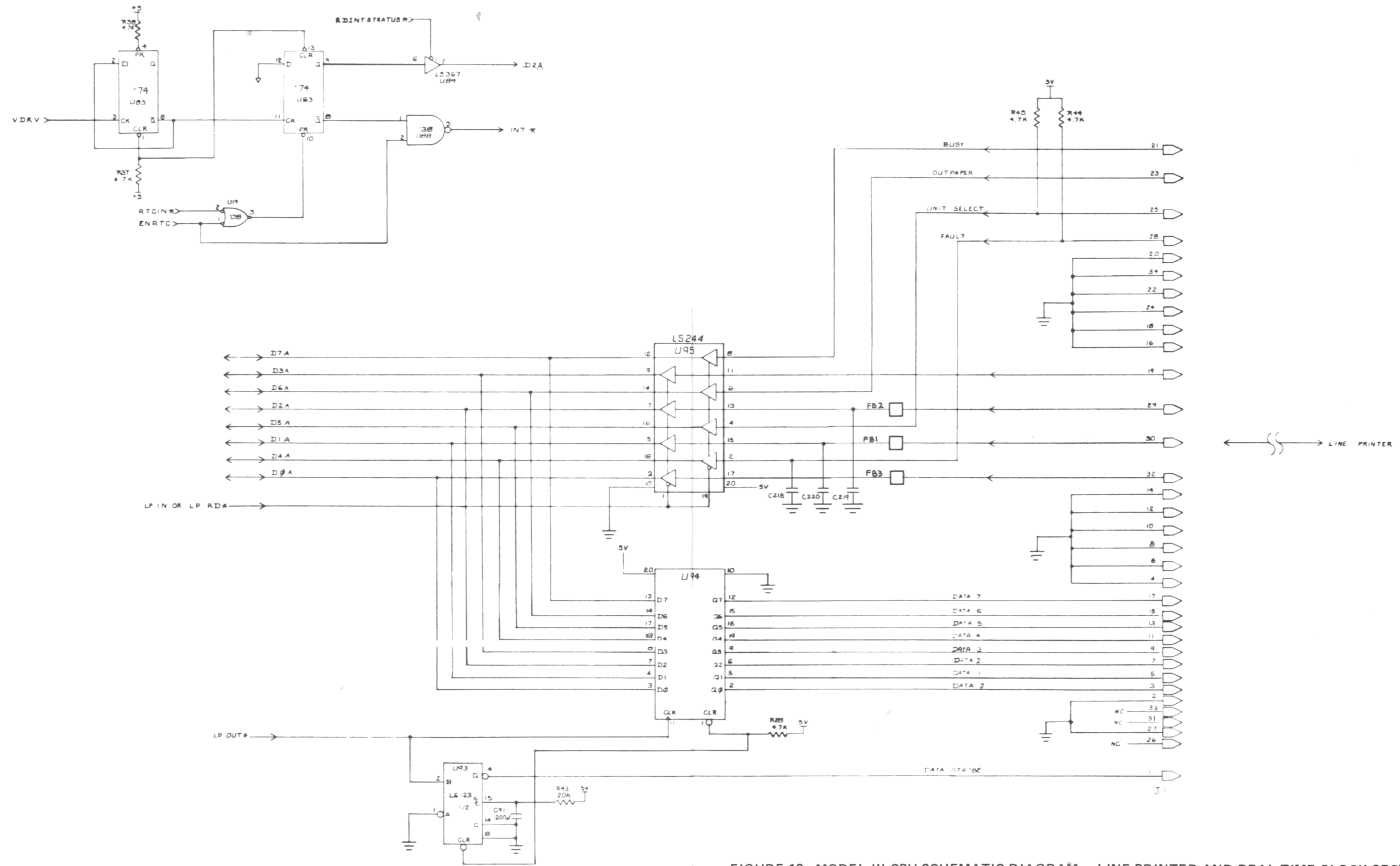


FIGURE 12. MODEL III CPU SCHEMATIC DIAGRAM – LINE PRINTER AND REAL TIME CLOCK SECTION

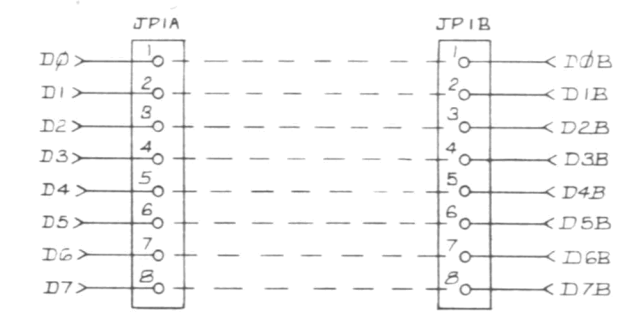
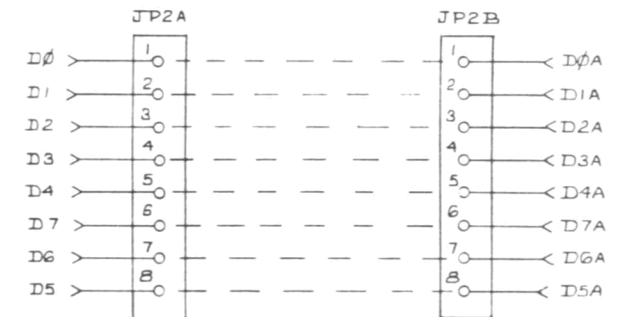
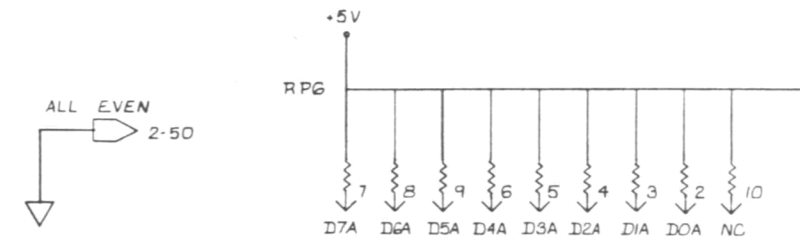
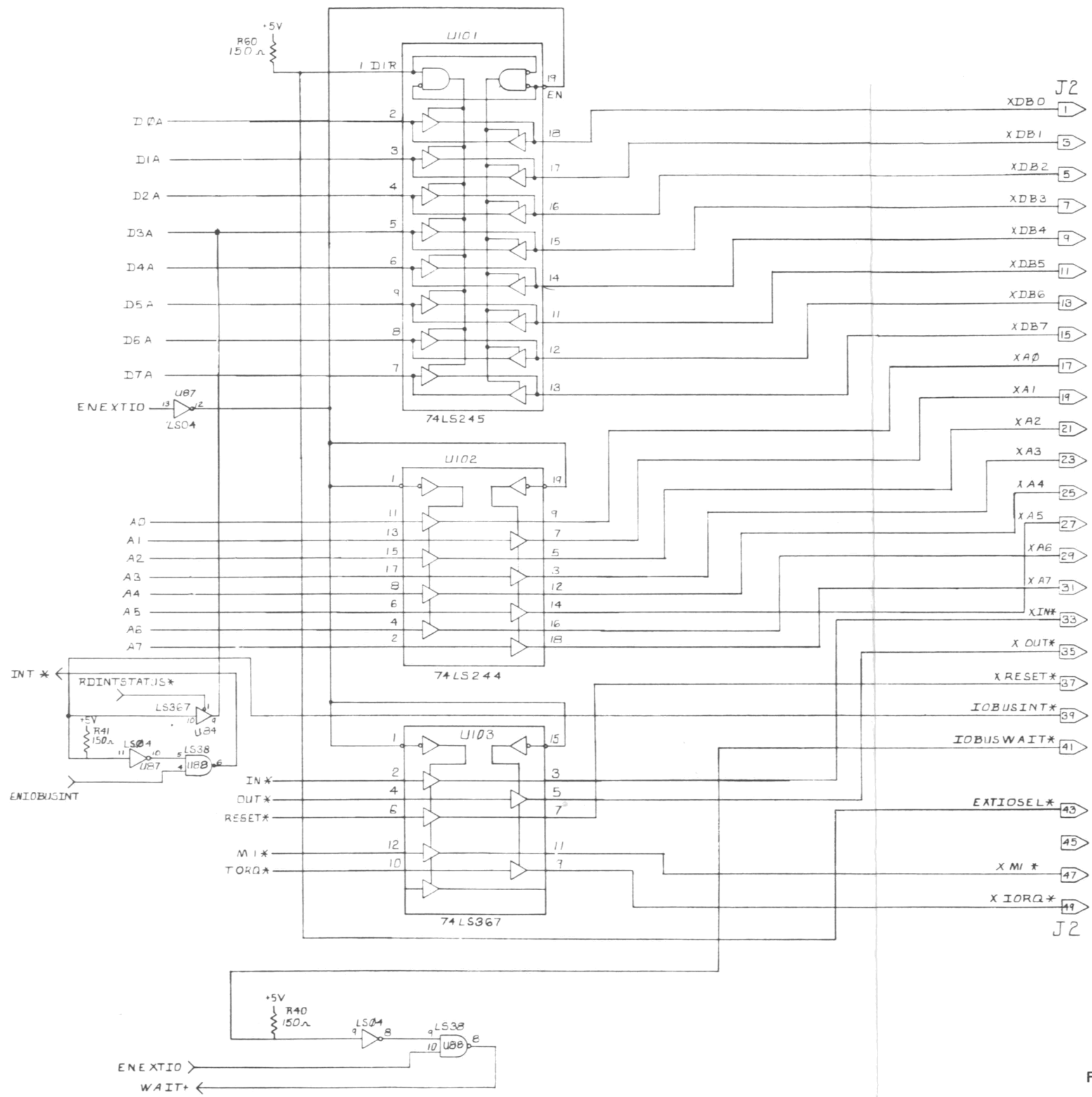


FIGURE 13. MODEL III CPU SCHEMATIC DIAGRAM - I/O BUS SECTION

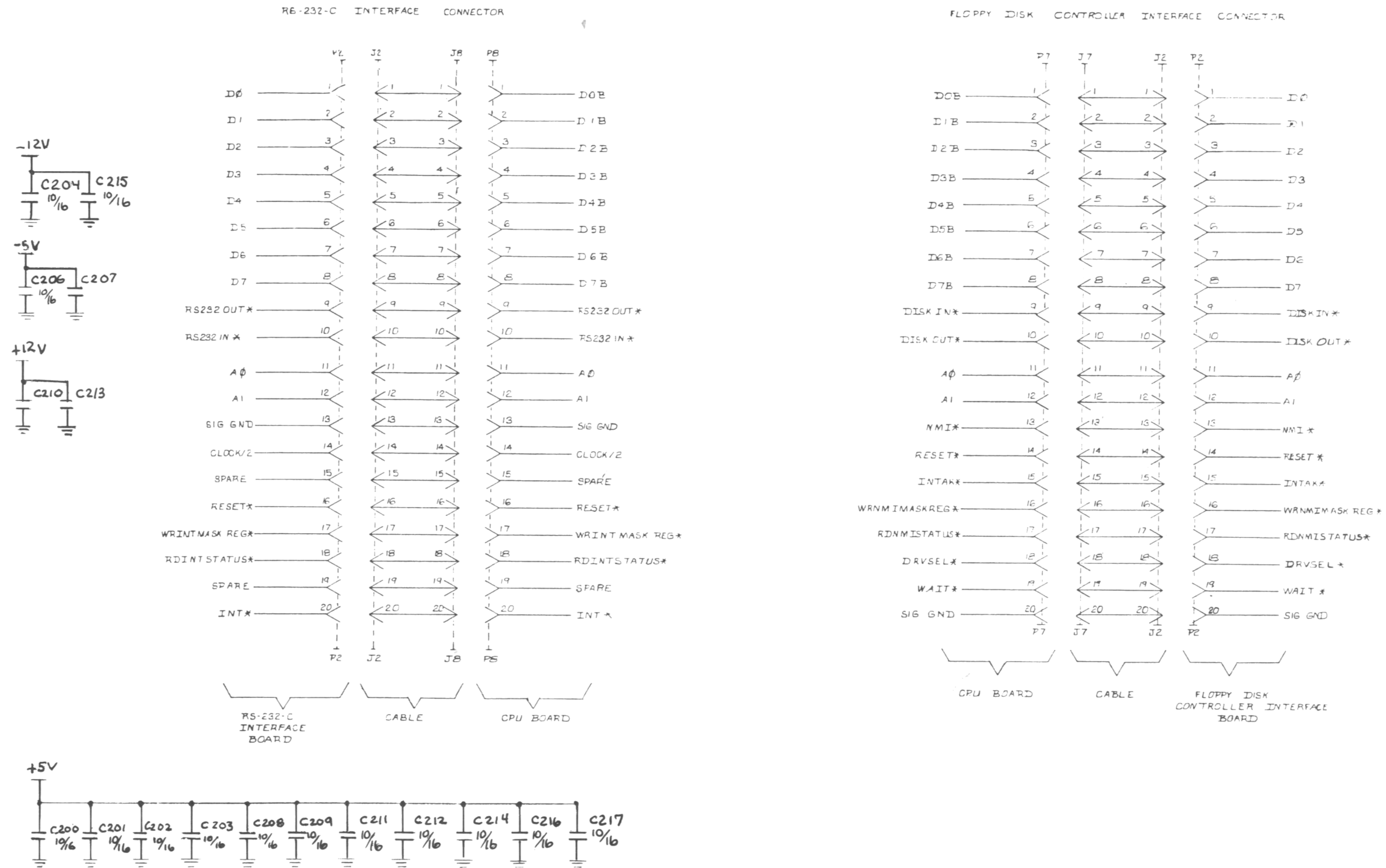


FIGURE 14. MODEL III CPU SCHEMATIC DIAGRAM – RS-232-C INTERFACE AND FDC INTERFACE CONNECTORS

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SECTION IV

FLOPPY DISK INTERFACE

TECHNICAL DESCRIPTION

The TRS-80 Model III Floppy Disk Interface Board is an optional board which if incorporated provides a standard five inch floppy disk controller. The Floppy Disk Interface Board supports both single and double density encoding schemes. This feature, along with a special software package, allows the transfer of Model I disk files to the Model III system. This results in an upgrade to double density encoding for the Model III owner. Write precompensation can be software enabled or disabled beginning at any track, although the system software enables write precompensation for all tracks greater than twenty-one. The amount of write precompensation is continuously variable from 0nsec to more than 500 nsec. The write precompensation is factory adjusted to 200 nsec. The data clock recovery logic incorporates a phase-locked loop oscillator which achieves state of the art reliability. One to four drives may be controlled by the interface (two internal drives and two external). All data transfers are accomplished by CPU data requests. In double density operation, data transfers are synchronized to the CPU by forcing a wait to the CPU and clearing the wait by a data request from the FDC chip. The end of the data transfer is indicated by generating a non-maskable interrupt from the interrupt request output of the FDC chip. A hardware watchdog timer insures that error conditions will not hang the wait line to the CPU for a period long enough to destroy RAM contents.

CONTROL AND DATA BUFFERING

Refer to the Schematic Diagram.

The Floppy Disk Controller Board is an I/O port mapped device which utilizes ports E4H, F0H, F1H, F2H, F3H, and F4H. The decoding logic is implemented on the CPU board. (See the Decoding Logic section of the CPU discussion.) U4 of the Floppy Disk Controller Board is a non-inverting octal buffer which isolates and buffers the required control signals. Table 1 summarizes the port and bit allocation for the Floppy Controller Board. U2 of the Floppy Disk Controller Board is a bi-directional, 8-bit transceiver used to buffer data to and from the Floppy Controller Board. The direction of data transfer is controlled by the combination of control signals DISKIN* and RDNMIMASKREG*. If either signal is active (logic low), U2 is enabled to drive data onto the CPU board data bus. If both signals are inactive (logic high), U2 is enabled to receive data from the CPU data bus.

NONMASKABLE INTERRUPT LOGIC

A dual "D" flip-flop (U5) is used to latch data bits D6 and D7 on the rising edge of the control signal WRNMIMASREG*. The outputs of U5 control the conditions which will generate a non-maskable interrupt to the CPU. The NMI interrupt conditions are programmed by doing an OUT instruction to port E4H with the appropriate bits set. If data

bit 7 is set, an NMI will be generated by an FDC interrupt request. If data bit 7 is reset, interrupt requests from the FDC are disabled. If data bit 6 is set, an NMI will be generated by Motor Time Out. If data bit 6 is reset, interrupts on Motor Time Out are disabled. An IN instruction from port E4H enables the CPU to question the Floppy Disk Controller Board to determine the source of the non-maskable interrupt. Data bit 7 indicates the status of FDC interrupt request (0 = true, 1 = false). Data bit 6 indicates the status of Motor Time Out (0 = true, 1 = false). Data bit 5 indicates the status of the front panel reset (0 = true, 1 = false). The control signal RDNMIMASKREG* when active (logic 0), gates this status onto the CPU data bus.

DRIVE SELECT LATCH AND MOTOR ON LOGIC

Selecting a drive prior to a disk I/O operation is accomplished by doing an OUT instruction to port F4H with the proper bit set. The following table describes the bit allocation of the Drive Select Latch.

| DATA BIT | FUNCTION |
|----------|---|
| D0 | Selects Drive 0 when set * |
| D1 | Selects Drive 1 when set * |
| D2 | Selects Drive 2 when set * |
| D3 | Selects Drive 3 when set * |
| D4 | Side 0 selected when reset, Side 1 selected if set |
| D5 | Write Precom. engaged when set, disabled if reset |
| D6 | Generate waits if set, no waits if reset |
| D7 | Selects MFM mode if set, FM mode if reset |

*Only one of these bits should be set per output.

A hex "D" flip-flop (U6) latches the drive select bits, side select and FM*/MFM bits on the rising edge of the control signal IDRVSEL*. A dual "D" flip-flop (U18) is used to latch the Wait Enable and Precompensation enable bits on the rising edge of IDRVSEL*. The rising edge of IDRVSEL* also triggers a one-shot (1/2 of U15) which produces a Motor On to the disk drives. The duration of the Motor On signal is approximately two seconds. The spindle motors are not designed for continuous operation, therefore the inactive state of the Motor On signal is used to clear the Drive Select Latch, which de-selects any drives which were previously selected. The Motor On one-shot is retriggerable by simply executing an OUT instruction to the Drive Select Latch.

WAIT STATE GENERATION AND WAITIMOUT LOGIC

As previously mentioned, a wait state to the CPU can be initiated by an output to the Drive Select Latch with D6 set. Pin 5 of U18 will go high after this operation. This signal is inverted by 1/6 of U1 and is routed to the CPU board where it forces the Z-80 into a wait state. The Z-80 will remain in the wait state as long as WAIT* is low. Once initiated, the wait state will remain until one of four conditions are satisfied. One half of U10 (a five input NOR gate) is used to perform this function. INTRQ, DRQ, RESET, and WAITIMOUT are the inputs to the NOR gate. If any one of these inputs are active (logic high), the output of the NOR gate (U10 pin 6) will go low. This output is tied to the clear input of the wait latch. This signal, when low, will clear the Q output (U18 pin 5) and set the Q* output (U18 pin 6). This condition causes WAIT* to go high and allows the Z-80 to exit the wait state. U20 is a 12-bit binary counter which serves as a watchdog timer to insure that a wait condition will not persist long enough to destroy dynamic RAM contents. The counter is clocked by a 1MHz signal and is enabled to count when its reset pin is low (U20 pin 11). A logic high on U20 pin 11 resets the counter outputs. U20 pin 15 is the divide by 1024 output and is used to generate the signal WAITIMOUT. This watchdog timer logic will limit the duration of a wait to 1024 μ sec, even if the FDC chip fails to generate a data request or an interrupt request.

CLOCK GENERATION LOGIC

A 4MHz crystal oscillator and a divide by 2 and divide by 4 counter generate the clock signals required by the FDC board. The basic 4MHz oscillator is implemented with two invertors (1/3 of U25) and a quartz crystal (Y1). One half of U24 is used to divide the basic 4MHz clock by 2 to produce a 2MHz output at U24 pin 6. This output is again divided by 2 using the remaining half of U24 to produce a 1MHz output at U24 pin 8. The 1MHz clock is used to drive the clock input of the 1793 FDC chip and the clock input of the watchdog time (U20).

DISK BUS SELECTOR LOGIC

As mentioned previously, the Model III Floppy Disk Board supports up to four drives (two internal, two external). This function is implemented by using two disk drive interface buses, one for the internal drives and one for the external drives. J4 is the edge connector used for the internal drives and J1 is the edge connector for the external drives. U22 (a quad 2 to 1 data selector) is used to select which set of inputs from the disk drive buses are routed to the 1793 FDC chip. U22 pin 1 is the control pin for the data selector. If U22 pin 1 is low, the external inputs are selected, otherwise the internal inputs are selected. This control signal (labeled EXTSEL*) is derived from the outputs of the Drive Select Latch. If Drive 2 or Drive 3 is selected, U17 pin 1

will go low indicating that an external drive is selected. One half of U10 (a five input NOR gate) is used to detect when any of the four drives are selected. The output of this NOR gate (U10 pin 5) is inverted and is used as the head load timing and ready signal for the 1793 FDC chip. Therefore if any drive is selected, the head is assumed to be loaded and the selected drive is assumed to be ready.

READ/WRITE DATA PULSE SHAPING LOGIC

Two one-shots (1/2 of U15 and 1/2 of U23) are used to insure that the read and write data pulses are approximately 450nsec in duration.

DISK BUS OUTPUT DRIVERS

High current open collector drivers (U21, U9, and U1) are used to buffer the output signals from the Drive Select Latch and the FDC chip to the floppy disk drives. Note from the schematic that each output signal to the drives has two buffers associated with each signal, one set is used for the internal drive bus and the other set is used for the external bus. No select logic is required for these output signals since the drive select bits define which drive is active.

WRITE PRECOMPENSATION AND CLOCK RECOVERY LOGIC

The Write Precompensation and Read Clock Recovery logic is comprised of U11 (WD1691), U13 (WD2143) and U14 (LS629), along with a few passive components. The WD1691 is an LSI device which minimizes the external logic required to interface the 1793 FDC chip to a disk drive. With the use of an external VCO, U14, the WD1691 will derive the RCLK signal for the 1793, while providing an adjustment signal for the VCO, to keep the RCLK synchronous with the read data from the drive. Write precompensation control signals are also provided by the WD1691 to interface directly to the WD2143 (U13) clock generator. The Read Clock Recovery section of the WD1691 has five inputs: DDEN*, VCO, RDD*, WG, and VFOE*/WF. It also has three outputs: PU, PD*, and RCLK. The inputs VFOE*/WF and WG when both are low, enable the Clock Recovery logic. When WG is high, a write operation is in progress and the Clock Recovery circuits are disabled regardless of the state of any other inputs.

The Write Precompensation section of the WD1691 was designed to be used with the WD2143 clock generator. Write Precompensation is not used in single density mode and the signal DDEN* when high indicates this condition. In double density mode (DDEN* = 0), the signals EARLY and LATE are used to select a phase input (01 - 04) on the leading edge of WDIN. The STB line is latched high when this occurs, causing the WD2143 to start its pulse generation.

02 is used as the write data pulse on nominal (EARLY = LATE = 0), 01 is used for the early, and 03 is used for the late. The leading edge of 04 resets the STB line in anticipation of the next write data pulse. When TG43 = 0 or DDEN* = 1, precompensation is disabled and any transitions on the WDIN line will appear on the WDOOUT line.

When VFOE*/WF and WG are low, the Clock Recovery circuits are enabled. When the RDD* line goes low, the PU or PD* signals will become active. If the RDD* has made its transition in the beginning of the RCLK window, PU will go from a high impedance state to a logic one, requesting an increase in VCO frequency. If the RDD* line has made its transition at the end of the RCLK window, PU will remain in the high impedance state while PD* will go to a logic zero, requesting a decrease in the VCO frequency. When the leading edge of RDD* occurs in the center of the RCLK window, both PU and PD* will remain in the high impedance state, indicating that no adjustment of the VCO frequency is required. By tying PU and PD* together, an adjustment signal is created which will be forced low for a decrease in VCO frequency and forced high for an increase in VCO frequency. To speed up rise times and stabilize the output voltage, a resistor divider using R7, R10, and R9 is used to adjust the tri-state level at approximately 1.4V. This adjustment results in a worst case voltage swing of plus or minus 1V, which is acceptable for the frequency control input of the VCO (U14). This signal derived from the combination of PU and PD* will eventually correct the VCO input to exactly the same frequency multiple as the FDD* signal. The leading edge of the RDD* signal will then occur in the exact center of the RCLK window, an ideal condition for the 1793 internal recovery circuits.

FLOPPY DISK CONTROLLER CHIP

The 1793 is an MOS LSI device which performs the functions of a floppy disk formatter/controller in a single chip implementation. The 1793 is functionally identical to the 1791 used on the Model II FDC Printer Interface Board, except that the data bus is true as opposed to inverted. Refer to the appendix section for more information on the FD1793. The Model II Technical Reference Manual also contains a good presentation of the 1791 FDC chip as well as a discussion on Write Precompensation. The following port addresses are assigned to the internal registers of the 1793 FDC chip.

| PORT # | FUNCTION |
|--------|-------------------------|
| F0H | Command/Status Register |
| F1H | Track Register |
| F2H | Sector Register |
| F3H | Data Register |

ADJUSTMENTS AND JUMPER OPTIONS

The Data Separator must be adjusted with the 1793 in an idle condition (no command currently in operation). Adjust R7 potentiometer for a 1.4V level on pin 2 of U14. Then adjust R6 potentiometer to yield a 2MHz square wave at pin 16 of U11.

The Write Precompensation must be adjusted while executing a continuous write command on a track greater than twenty-one. Adjust R5 potentiometer to yield 200nsec wide pulses at pin 4 of U11. This results in a write precompensation value of 200nsec.

There are four jumper options on the Floppy Disk Controller Board. They are designated on the PC Board silkscreen and are referenced on the Schematic Diagram. The jumpers should be installed as described below.

JUMPER CONNECTIONS

A to B
E to G
L to M
H to J

FLOPPY DISK CONTROLLER INTERFACE CONNECTOR

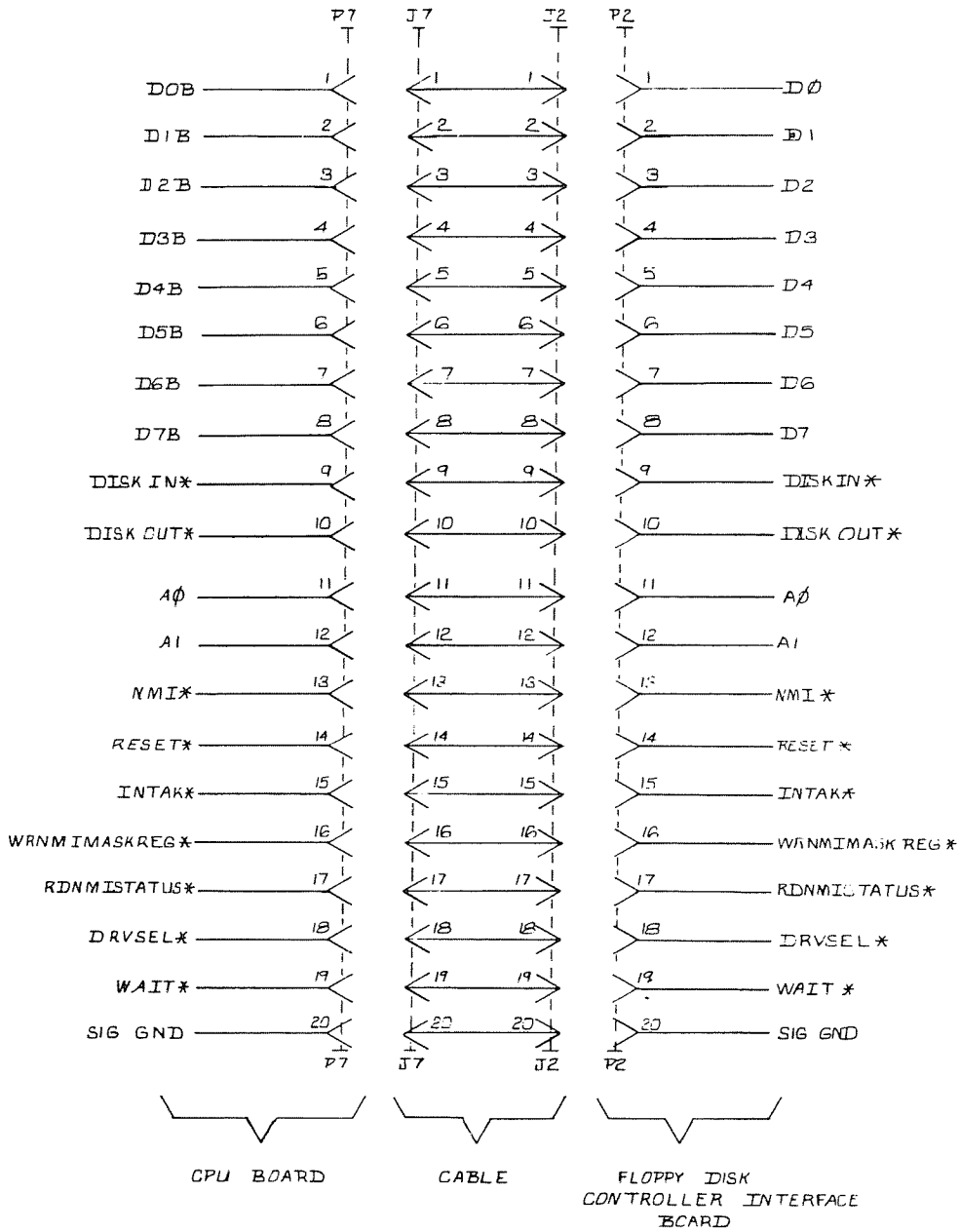


FIGURE 1. FDC BOARD TO CPU BOARD SIGNAL DESCRIPTION

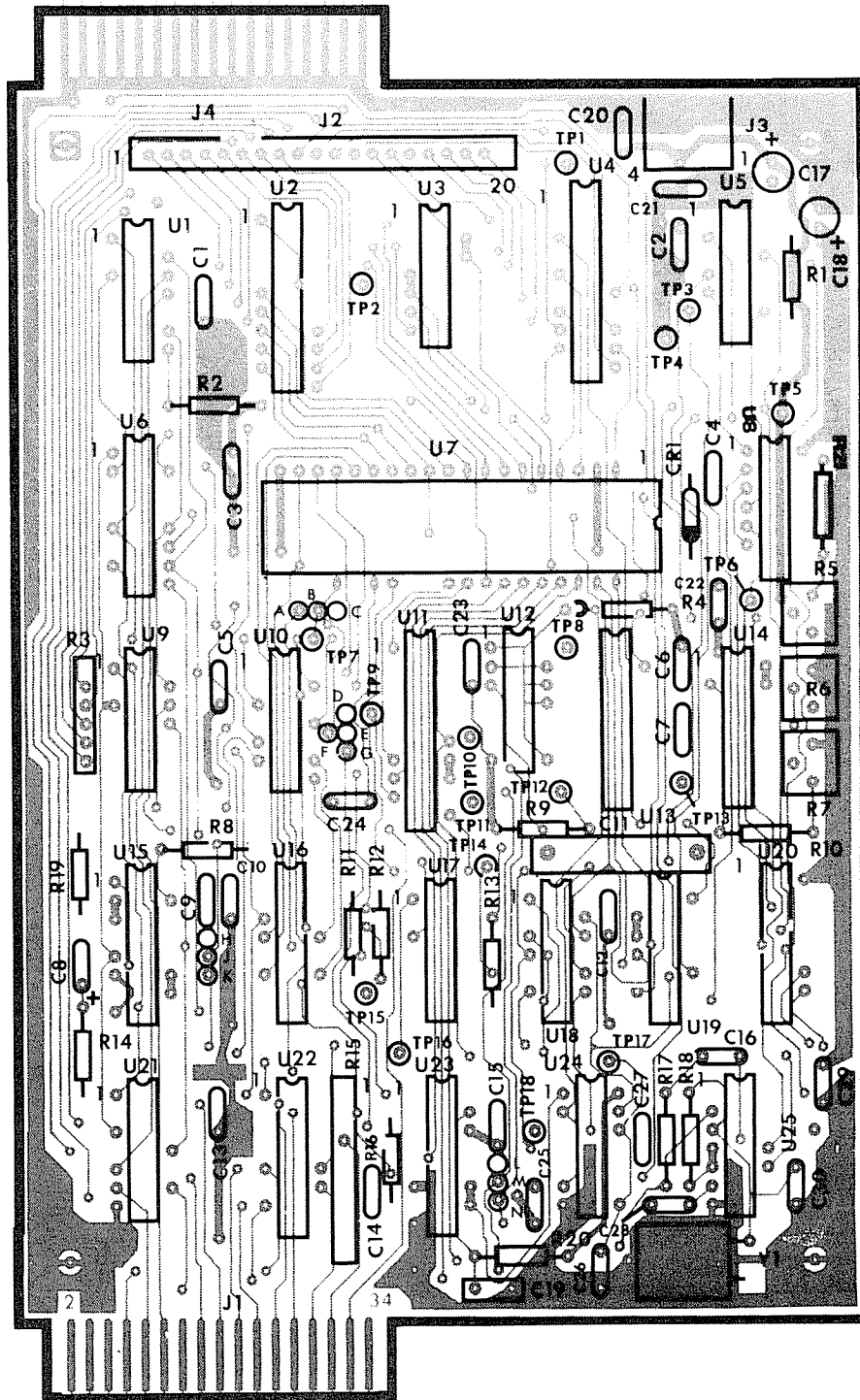


FIGURE 2. FLOPPY DISK INTERFACE PC BOARD – COMPONENT SIDE

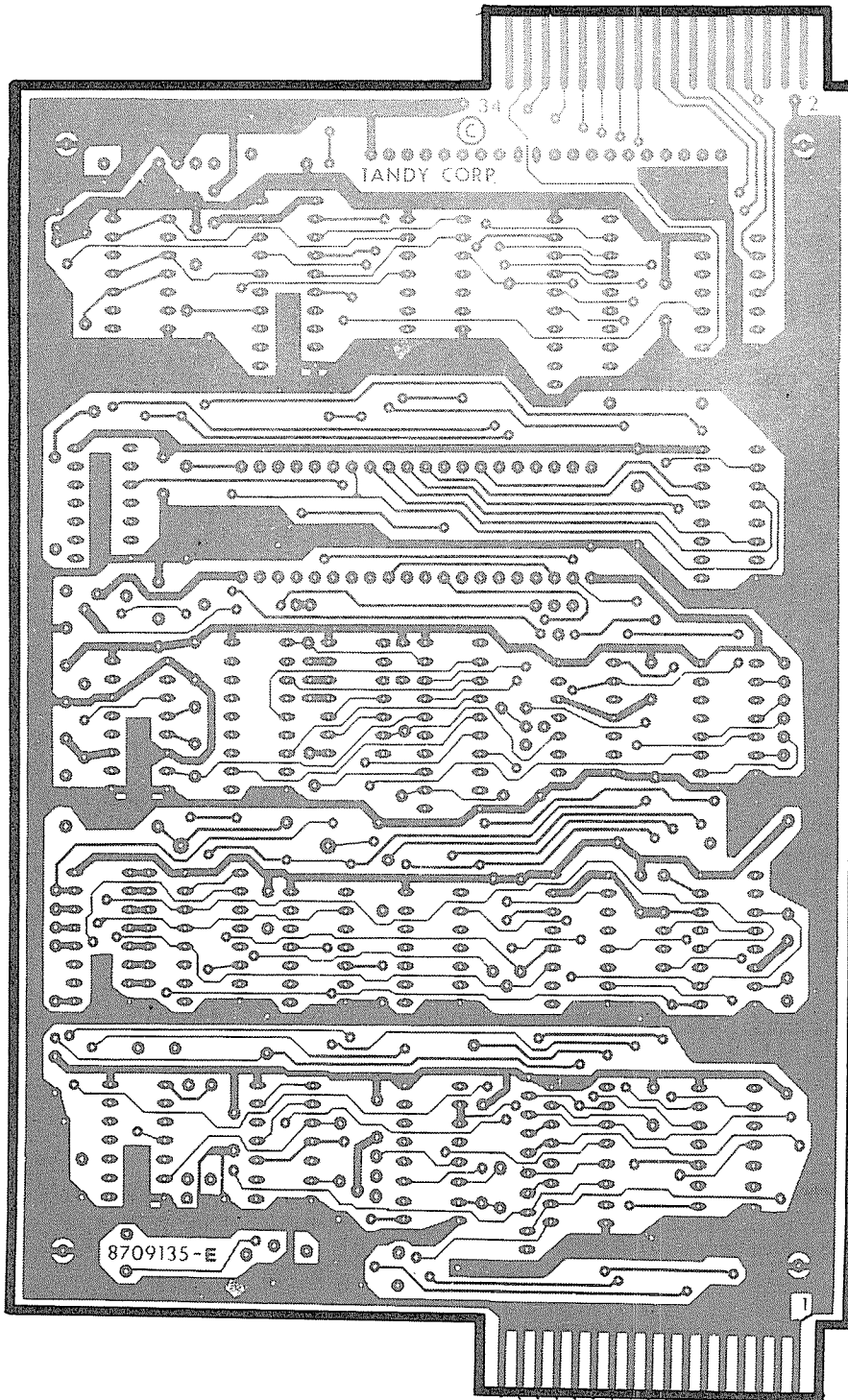


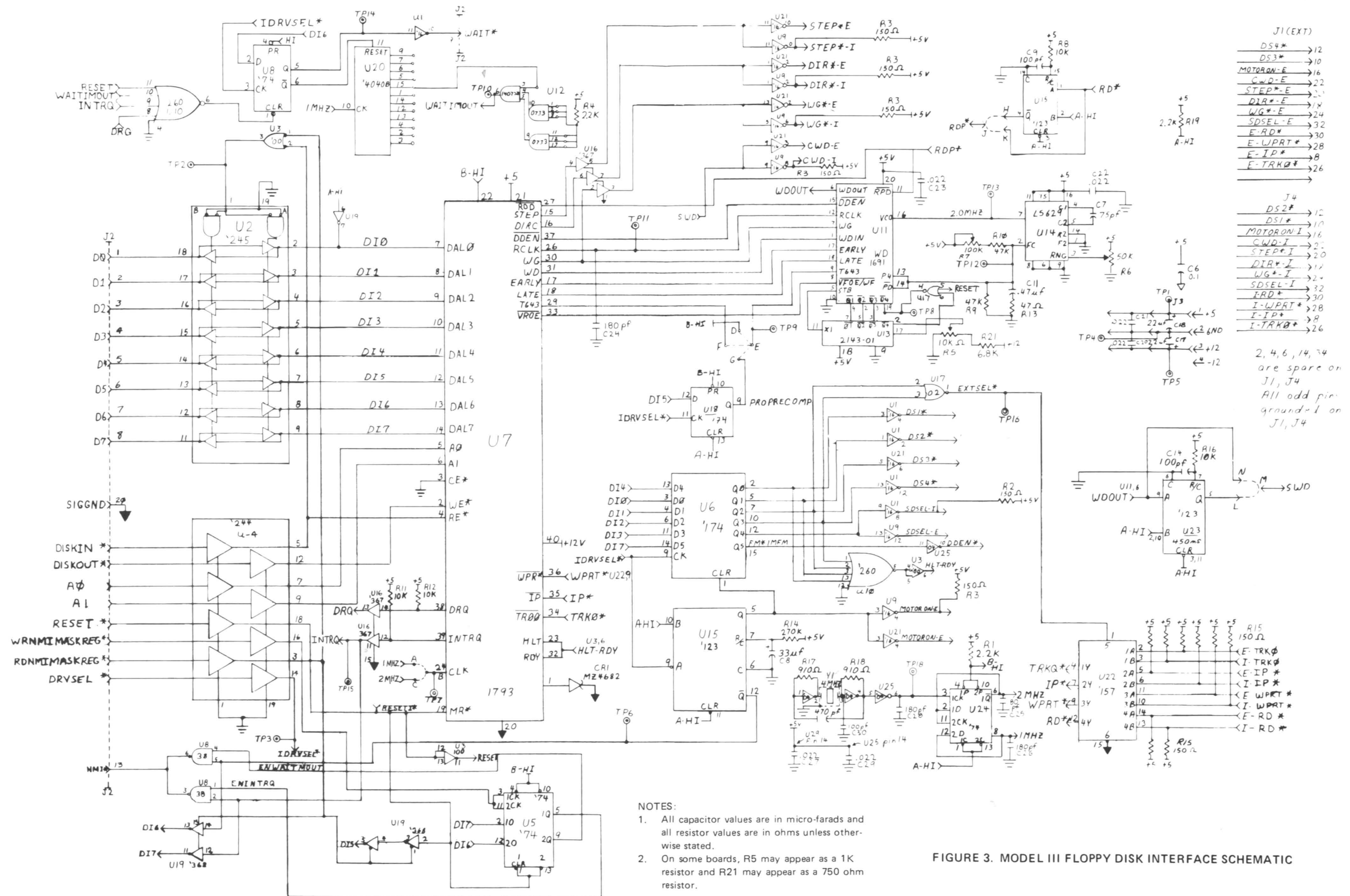
FIGURE 2. FLOPPY DISK INTERFACE PC BOARD – CIRCUIT SIDE

FLOPPY DISK INTERFACE PC BOARD PARTS LIST

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------------|---------------------------------------|-------------------------------|----------------------------|
| CAPACITORS | | | |
| C1 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C2 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C3 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C4 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C5 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C6 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C7 | 75pF, 50V, ceramic disc | 830-0754 | ----- |
| C8 | 33 μ F, 16V, electrolytic, radial | 839-6331 | ACC336QDAP |
| C9 | 100pF, 50V, ceramic disc | 830-1104 | ACC101QJCP |
| C10 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C11 | 0.47 μ F, 16V, mylar | 835-4471 | ----- |
| C12 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C13 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C14 | 100pF, 50V, ceramic disc | 830-1104 | ACC101QJCP |
| C15 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C16 | 470pF, 50V, ceramic disc | 830-1474 | ACC471QJCP |
| C17 | 10 μ F, 16V, electrolytic, radial | 832-6101 | ACC106QDAP |
| C18 | 10 μ F, 16V, electrolytic, radial | 832-6101 | ACC106QDAP |
| C19 | 0.01 μ F, 16V, ceramic disc | 830-3104 | ACC103QJCP |
| C20 | 0.022 μ F, 50V, ceramic disc | 830-3224 | ACC223QJCP |
| ↓ | ↓ | ↓ | ↓ |
| C23 | 0.022 μ F, 50V, ceramic disc | 830-3224 | ACC223QJCP |
| C24 | 180pF, ceramic disc | 830-1184 | ----- |
| C25 | 180pF, ceramic disc | 830-1184 | ----- |
| C26 | 180pF, ceramic disc | 830-1184 | ----- |
| C27 | 0.022 μ F, ceramic disc | 830-3224 | ACC223QJCP |
| C28 | 180pF, ceramic disc | 830-1184 | ----- |
| C29 | 0.022 μ F, ceramic disc | 830-3224 | ACC223QJCP |
| C30 | 100pF, ceramic disc | 830-1104 | ACC101QJCP |
| CONNECTORS | | | |
| J2 | 20 pos. right angle | 851-9078 | ----- |
| J3 | 4 pin right angle header | 851-9079 | AJ6977 |
| CRYSTAL | | | |
| Y1 | 4 MHz | 840-9010 | AMX2804 |
| DIODES | | | |
| CR1 | MZ4682 | 815-0682 | ADX1518 |
| INTEGRATED CIRCUITS | | | |
| U1 | 7416, Hex Inverter/Buffer | 800-0016 | ----- |
| U2 | 74LS245 | 802-0245 | AMX4470 |
| U3 | 74LS00, NAND gate | 802-0000 | AMX3550 |
| U4 | 74LS244, Octal Buffer | 802-0244 | AMX3864 |
| U5 | 74LS74, Dual "D" Flip-Flop | 802-0074 | AMX3558 |

FLOPPY DISK INTERFACE PC BOARD PARTS LIST

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|------------------------------|----------------------------------|-------------------------------|----------------------------|
| INTEGRATED CIRCUITS (cont'd) | | | |
| U6 | 74LS174, Quad "D" Flip-Flop | 802-0174 | AMX3565 |
| U7 | WD1793 | 850-9002 | AXX3041 |
| U8 | 74LS38, NAND Buffer | 802-0038 | AMX4328 |
| U9 | 7416, Hex Inverter/Buffer | 800-0016 | ----- |
| U10 | 74LS260, Dual NOR gate | 802-0260 | ----- |
| U11 | WD1691 | 850-9009 | AMX4471 |
| U12 | MC140733, AND gate | 803-0073 | ----- |
| U13 | WD2143-01 | 850-9006 | AMX4472 |
| U14 | 74LS629, VCO | 802-0629 | AMX4663 |
| U15 | 74LS123, Mono Multivibrator | 802-0123 | AMX3803 |
| U16 | 74LS367, Hex Buffer | 802-0367 | AMX3567 |
| U17 | 74LS02, NAND gate | 802-0002 | AMX3551 |
| U18 | 74LS74, Dual "D" Flip-Flop | 802-0074 | AMX3558 |
| U19 | 74LS368, Hex Inverter/Buffer | 802-0368 | AMX3568 |
| U20 | MC14040B, Binary Counter | 803-0040 | AMX4666 |
| U21 | 7416, Hex Inverter/Buffer | 800-0016 | ----- |
| U22 | 74LS157, Quad Multiplexer | 802-0157 | AMX3563 |
| U23 | 74LS123, Mono Multiplexer | 802-0123 | AMX3803 |
| U24 | 74LS74, Dual "D" Flip-Flop | 802-0074 | AMX3558 |
| U25 | 74LS04, Hex Inverter | 802-0004 | AMX3552 |
| RESISTORS | | | |
| R1 | 2.2K, 1/4W, 5% | 820-7222 | AN0216EEC |
| R2 | 150 ohm, 1/4W, 5% | 820-7115 | AN0142EEC |
| R3 | 150 ohm, 6 pin resistor network | 829-0012 | ARX0241 |
| R4 | 2.2K, 1/4W, 5% | 820-7222 | AN0216EEC |
| R5 | 1K, Trim Pot | 827-9210 | AP0835 |
| R6 | 50K, Trim Pot | 827-9350 | AP7168 |
| R7 | 100K, Trim Pot | 827-9410 | ----- |
| R8 | 10K, 1/4W, 5% | 820-7310 | AN0281EEC |
| R9 | 47K, 1/4W, 5% | 820-7347 | AN0340EEC |
| R10 | 47K, 1/4W, 5% | 820-7347 | AN0340EEC |
| R11 | 10K, 1/4W, 5% | 820-7310 | AN0281EEC |
| R12 | 10K, 1/4W, 5% | 820-7310 | AN0281EEC |
| R13 | 47 ohm, 1/4W, 5% | 820-7047 | AN0099EEC |
| R14 | 270K, 1/4W, 5% | 820-7427 | ----- |
| R15 | 150 ohm, 10 pin resistor network | 829-0013 | ARX0242 |
| R16 | 10K, 1/4W, 5% | 820-7310 | AN0281EEC |
| R17 | 910 ohm, 1/4W, 5% | 820-7191 | AN0192EEC |
| R18 | 910 ohm, 1/4W, 5% | 820-7191 | AN0192EEC |
| R19 | 2.2K, 1/4W, 5% | 820-7222 | AN0216EEC |
| R20 | 22K, 1/4W, 5% | 820-7322 | ----- |
| MISCELLANEOUS | | | |
| | Socket, 18 pin | 850-9006 | AJ6701 |
| | Socket, 20 pin | 850-9009 | AJ6760 |
| | Socket, 40 pin | 850-9002 | AJ6580 |
| | FDC Board, complete assembly | | AXX0510 |
| | FDC Board, without major chips | | AXX0509 |



- NOTES:
1. All capacitor values are in micro-farads and all resistor values are in ohms unless otherwise stated.
 2. On some boards, R5 may appear as a 1K resistor and R21 may appear as a 750 ohm resistor.

FIGURE 3. MODEL III FLOPPY DISK INTERFACE SCHEMATIC

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SECTION V

RS-232C CIRCUIT BOARD



RS-232C TECHNICAL DESCRIPTION

The RS-232C option board for the Model III computer supports asynchronous serial transmissions and conforms to the EIA RS-232C standards at the input - output interface (P1). The heart of the board is the TR1602 Asynchronous Receiver/Transmitter. It performs the job of converting the parallel byte data from the CPU to a serial data stream including start, stop, and parity bits. For a more detailed description of how this LSI circuit performs these functions, refer to the TR1602 data sheets and application notes. The transmit and receive clock rates that the TR1602 needs are supplied by the Baud rate generator (BR19411). This circuit takes the 5.0688 MHz supplied by the CPU board and the programmed information received from the CPU over the data bus and divides the basic clock rate to provide two clocks. The rates available from the BRG go from 50 Baud to 19200 Baud. See the BRG table for the complete list.

BRG PROGRAMMING TABLE

| NIBBLE LOADED | TRANSMIT OR RECEIVE BAUD RATE | 16X CLOCK FREQUENCY | SUPPORTED BY SETCOM |
|---------------|----------------------------------|---------------------|------------------------|
| 0H | 50 | 0.8 kHz | yes |
| 1H | 75 | 1.2 kHz | yes |
| 2H | 110 | 1.76 kHz | yes |
| 3H | 134.5 | 2.1523 kHz | yes |
| 4H | 150 | 2.4 kHz | yes |
| 5H | 300 | 4.8 kHz | yes |
| 6H | 600 | 9.6 kHz | yes |
| 7H | 1200 | 19.2 kHz | yes |
| 8H | 1800 | 28.8 kHz | yes |
| 9H | 2000 | 32.081 kHz | yes |
| AH | 2400 | 38.4 kHz | yes |
| BH | 3600 | 57.6 kHz | yes |
| CH | 4800 | 76.8 kHz | yes |
| DH | 7200 | 115.2 kHz | yes |
| EH | 9600 | 113.6 kHz | yes |
| FH | 19,200 | 316.8 kHz | yes |

The RS-232C board is a port mapped device and the ports used are E8 to EB. Following is a description of each port on both input and output.

| PORT | INPUT | OUTPUT |
|------|------------------------------|--|
| E8 | Modem status | Master Reset, enables UART control register load |
| EA | UART status | UART control register load and modem control |
| E9 | Not Used | Baud rate register load enable bit |
| EB | Receiver Holding register | Transmitter Holding register |

The following list is a pinout description of the DB-25 connector (P1).

| PIN# | SIGNAL |
|------|---------------------------|
| 1 | PGND (Protective Ground) |
| 2 | TD (Transmit Data) |
| 3 | RD (Receive Data) |
| 4 | RTS (Request To Send) |
| 5 | CTS (Clear To Send) |
| 6 | DSR (Data Set Ready) |
| 7 | SGND (Signal Ground) |
| 8 | CD (Carrier Detect) |
| 20 | DTR (Data Terminal Ready) |
| 22 | RI (Ring Indicate) |

Interrupts are supported on the RS-232C option board by the Interrupt mask register (U10) and the Status register (U9) which allows the CPU to see which kind of interrupt has occurred. Interrupts can be generated on receiver data register full, transmitter register empty, and any one of the errors — parity, framing, or data overrun. This allows a minimum of CPU overhead in transferring data to or from the UART. The interrupt mask register is port E0 (write) and the interrupt status register is port E0 (read). Refer to the IO Port description for a full breakdown of all interrupts and their bit positions.

The Model III RS-232C board is functionally identical to the Model I RS-232 board with the following exceptions:

Interrupts are supported, there are no sense switches for configuring the interface, there is no COM/TERM switch for reversing the function of pins 2 and 3 on the DB-25, and the DC to DC converter is not required since +12V and -12V are provided by the internal power supply. Other differences include three additional interface outputs and no crystal for the BRG. All Model I software written for the RS-232 interface is compatible with the Model III RS-232C option board, provided that the software does not use the sense switches to configure the interface. The programmer can get around this problem by directly programming the BRG and UART for the desired configuration or by using the SETCOM command of the disk operating system to configure the interface. The TRS-80 RS-232C Interface hardware manual has a good discussion of the RS-232C standard and specific programming examples (Catalog Number 26-1145).

PORT AND BIT ASSIGNMENTS

PORT E8H

OUTPUT: MASTER RESET

INPUT: MODEM STATUS REGISTER

An output to this port (and data), performs a master reset to the UART and enables the control register load enable bit. The following table details the bit definitions for an input from port E8H.

| DATA BIT | FUNCTION |
|----------|-----------------------------------|
| D7 | Clear To Send, Pin 5 DB-25 |
| D6 | Data Set Ready, Pin 6 DB-25 |
| D5 | Carrier Detect, Pin 8 DB-25 |
| D4 | Ring Indicator, Pin 22 DB-25 |
| D3 | Not Used |
| D2 | Not Used |
| D1 | Not Used |
| D0 | Receiver Input, UART Pin 20 DB-25 |

PORT E9H

OUTPUT: BAUD RATE LOAD

INPUT: NOT USED

An output to this port loads the Baud rate generator with a code which corresponds to the desired receive and transmit Baud rate as outlined in the BRG Programming Table. The low order nibble of the data output to this port determines the receiver Baud rate, while the high order nibble determines the transmit Baud rate.

PORT EAH

OUTPUT: UART AND MODEM CONTROL

INPUT: UART STATUS

An output to this port loads the UART Control register if the enable bit for this function is set (D1 port E8H = 1). The UART Control register is five bits wide (D7 - D3) leaving three bits for modem control (D2 - D0). Three more modem control bits were added by allowing software to enable or disable the UART Control register. The tables below summarize the bit allocations with the UART Control register enabled and disabled.

PORT EAH OUTPUT BITS WITH UART CONTROL REGISTER ENABLED

| DATA BIT | FUNCTION |
|----------|--|
| D7 | Even Parity Enable, 1 = even, 0 = odd |
| D6 | Word Length Select 1 |
| D5 | Word Length Select 2 |
| D4 | Stop Bit Select, 1 = two stop bits, 0 = one stop bit |
| D3 | Parity Inhibit, 1 = disable parity |
| D2 | Break 0 = disable transmit data (continuous space) |
| D1 | Data Terminal Ready, Pin 20 DB-25 |
| D0 | Request To Send, Pin 4 DB-25 |

PORT EAH OUTPUT BITS WITH UART CONTROL REGISTER DISABLED

| DATA BIT | FUNCTION |
|---------------|--|
| D7 | Not Used |
| D6 | Not Used |
| D5 | Secondary unassigned, Pin 18 DB-25 |
| D4 | Secondary Transmit Data, Pin 14 DB-25 |
| D3 | Secondary Request To Send, Pin 19 DB-25 |
| D2 | Break \emptyset = disable Transmit Data (continuous space) |
| D1 | Data Terminal Ready, Pin 20 DB-25 |
| D \emptyset | Request To Send, Pin 4 DB-25 |

PORT EAH INPUT BITS

| DATA BITS | FUNCTION |
|---------------|--|
| D7 | Data Received, 1 = condition true |
| D6 | Transmitter Holding register empty, 1 = condition true |
| D5 | Overrun error, 1 = condition true |
| D4 | Framing error, 1 = condition true |
| D3 | Parity error, 1 = condition true |
| D2 | Not Used |
| D1 | Not Used |
| D \emptyset | Not Used |

PORT EBH

OUTPUT: TRANSMITTER HOLDING REGISTER

INPUT: RECEIVER HOLDING REGISTER

An output to this port loads the UART Transmitter Holding register with a word to be transmitted, as soon as the last word loaded in the holding register is transmitted. This register should never be loaded until the Transmitter Holding register empty bit (port EAH) is true. An input from this port reads the last word received from the UART received data holding register. This register should not be read until the data received bit (port EAH) is true.

RS-232-C INTERFACE CONNECTOR

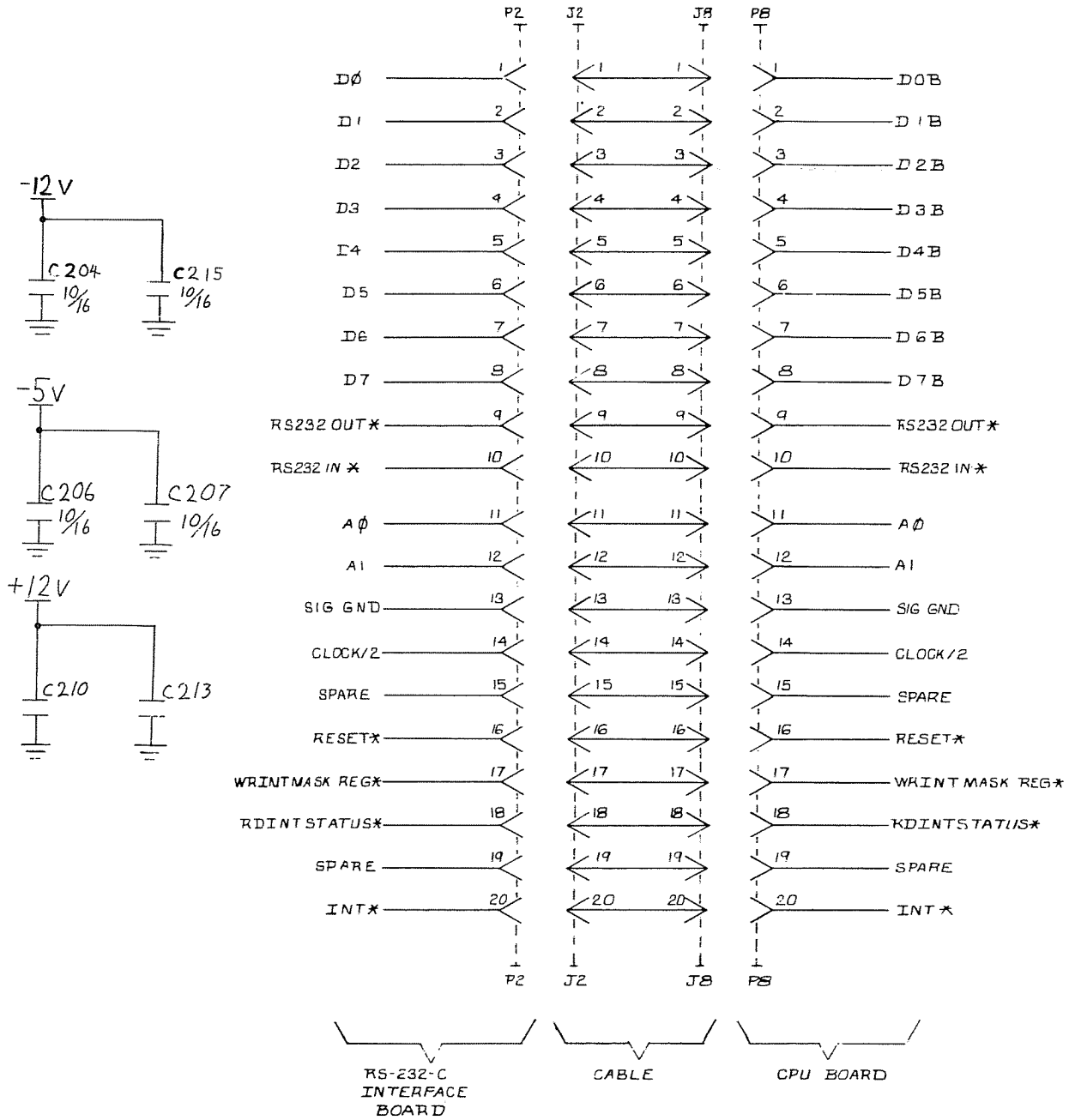


FIGURE 1. RS-232 BOARD TO CPU BOARD SIGNAL DESCRIPTION

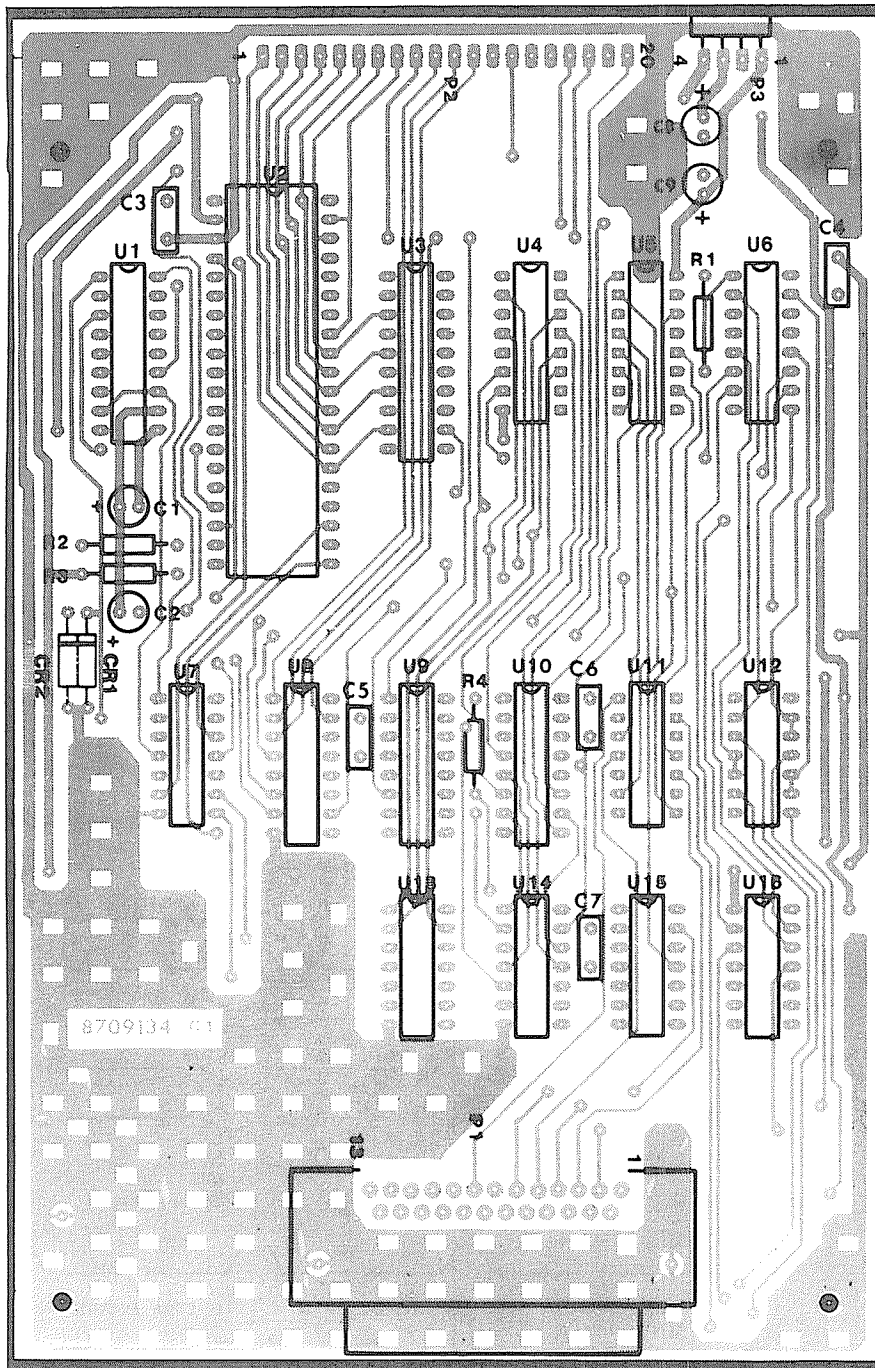


FIGURE 2. RS-232C PC BOARD – COMPONENT SIDE

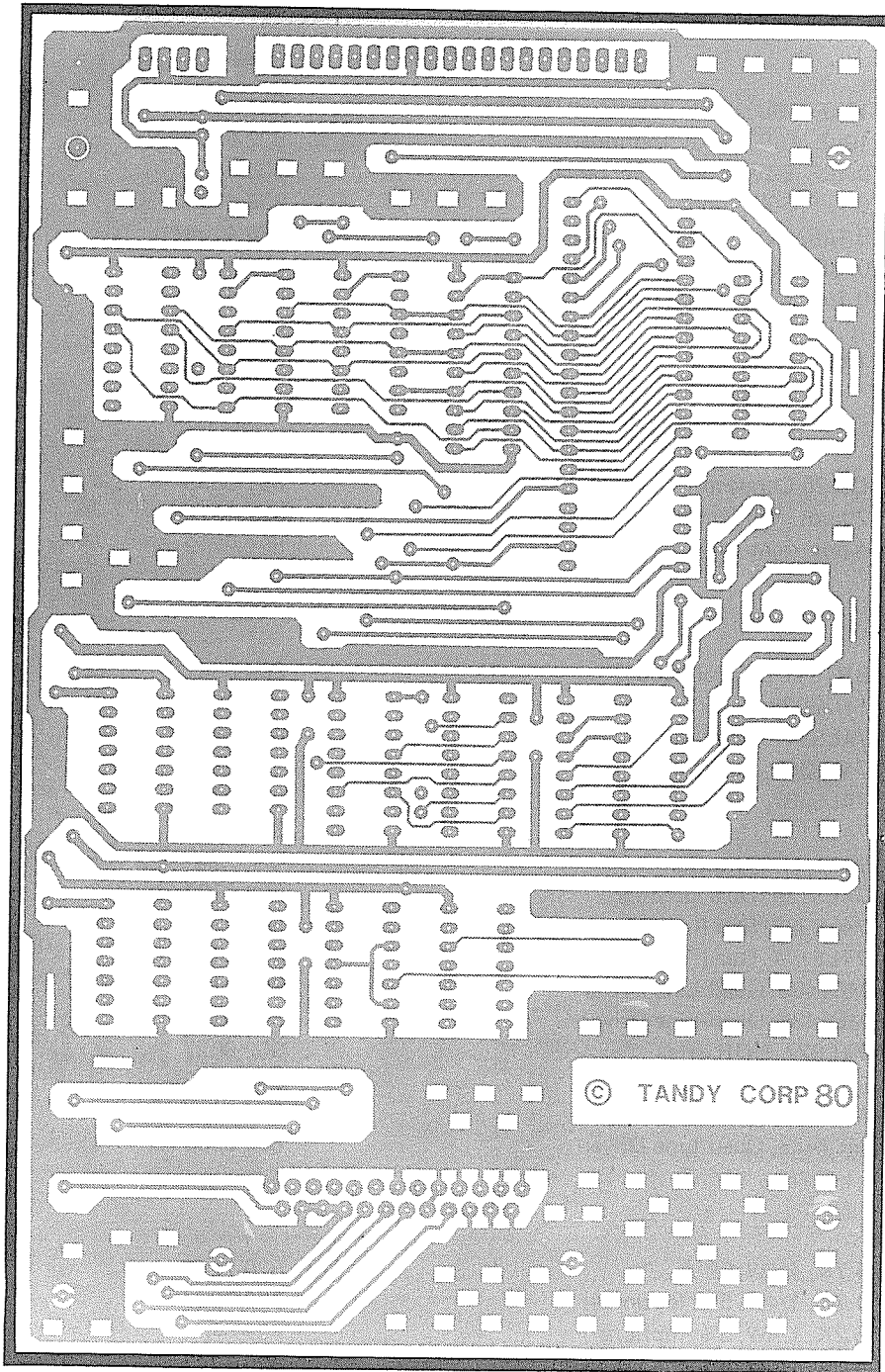


FIGURE 2. RS-232C PC BOARD – CIRCUIT SIDE

RS-232C PC BOARD PARTS LIST

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------------|--------------------------------------|-------------------------------|----------------------------|
| CAPACITORS | | | |
| C1 | 10 μ F, 16V, radial (optional) | 832-6101 | ACC106QDAP |
| C2 | 10 μ F, 16V, radial (optional) | 832-6101 | ACC106QDAP |
| C3 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C4 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C5 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C6 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C7 | 0.1 μ F, 50V, monolithic, radial | 838-4104 | ACC104QJAP |
| C8 | 10 μ F, 16V, radial | 832-6101 | ACC106QDAP |
| C9 | 10 μ F, 16V, radial | 832-6101 | ACC106QDAP |
| CONNECTORS | | | |
| P1 | DB-25 Connector | 851-9030 | ----- |
| P2 | 20 pos. right angle | 851-9078 | ----- |
| P3 | 4 pos. right angle | 851-9079 | AJ6977 |
| INTEGRATED CIRCUITS | | | |
| U1 | BR1941-L, Dual Baud C | 804-6941 | AMX3921 |
| U2 | TR1602B, UART | 804-5602 | AMX3865 |
| U3 | 74LS244, Octal Buffer | 802-0244 | AMX3864 |
| U4 | 74LS367, Hex Buffer | 802-0367 | AMX3567 |
| U5 | 74LS367, Hex Buffer | 802-0367 | AMX3567 |
| U6 | 74LS174, Quad "D" Flip-Flop | 802-0174 | AMX3565 |
| U7 | 7404, Hex Inverter | ----- | AMX3655 |
| U8 | 74LS139, Dual Decoder | 802-0139 | AMX3800 |
| U9 | 74LS368, Hex Buffer | 802-0368 | AMX3568 |
| U10 | 74LS174, Quad "D" Flip-Flop | 802-0174 | AMX3565 |
| U11 | MC1489, Quad Line Driver | 805-0189 | AMX3868 |
| U12 | MC1488, Quad Line Driver | 805-0188 | AMX3867 |
| U13 | 74LS27, NOR gate | 802-0027 | ----- |
| U14 | 74LS38, NAND Buffer | 802-0038 | AMX4328 |
| U15 | MC1489, Quad Line Driver | 805-0189 | AMX3868 |
| U16 | MC1488, Quad Line Driver | 805-0188 | AMX3867 |
| RESISTORS | | | |
| R1 | 4.7K, 1/4W, 5% | 820-7247 | AN0247EEC |
| R2 | 4.7K, 1/4W, 5% (optional) | 820-7247 | AN0247EEC |
| R3 | 6.2K, 1/4W, 5% (optional) | ----- | AMX4658 |
| R4 | 4.7K, 1/4W, 5% | 820-7247 | AN0247EEC |
| MISCELLANEOUS | | | |
| | Cable, 20 pos., 4.5", flat | 845-9020 | AW2631 |
| | Socket, 18 pin | 850-9006 | AJ6701 |
| | Socket, 40 pin | 850-9002 | AJ6580 |

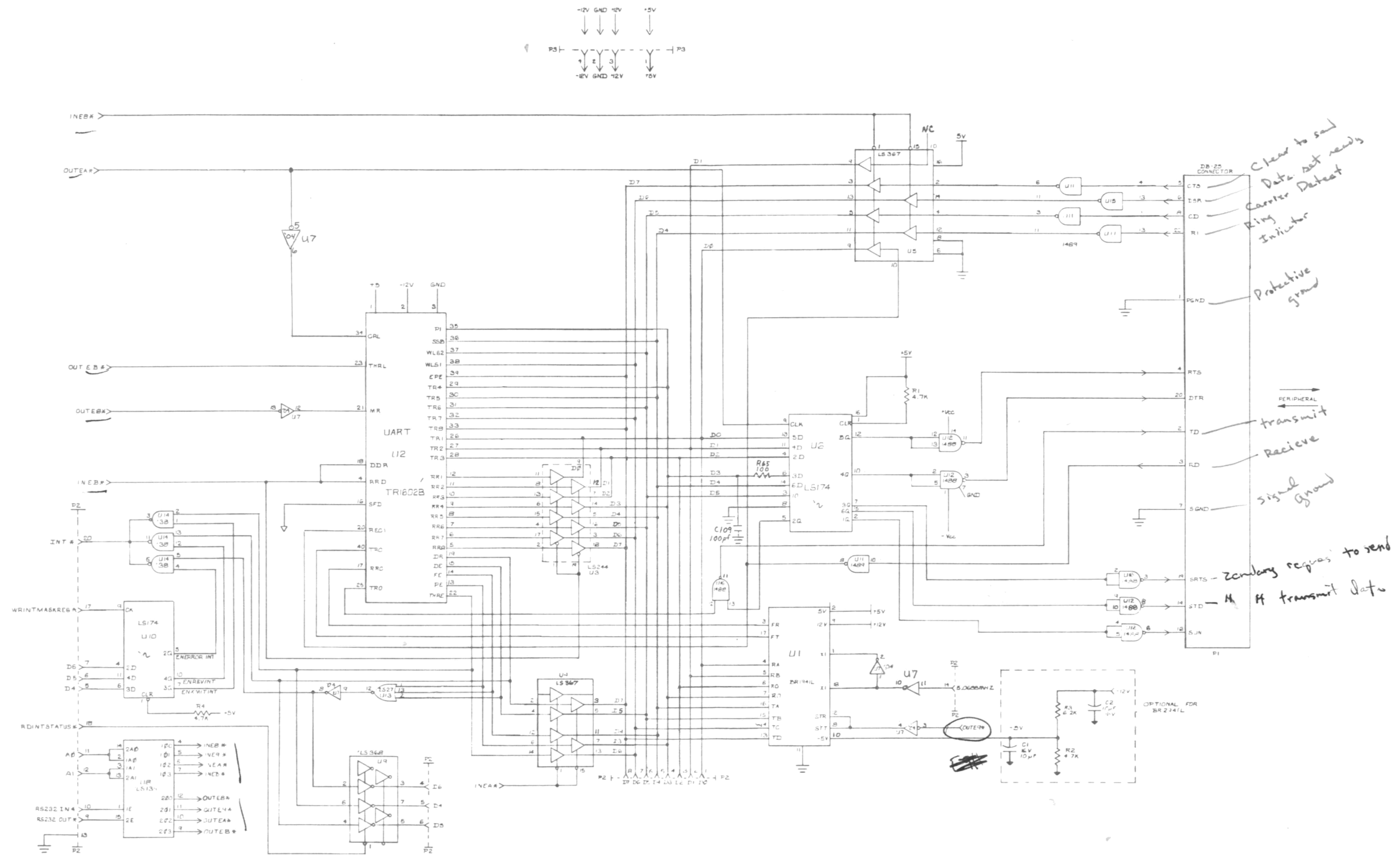


FIGURE 3. MODEL III RS-232C SCHEMATIC DIAGRAM

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SECTION VI

POWER SUPPLY

GENERAL

The power supply used in the Model III is a switch mode power supply utilizing the flyback method of power conversion. This supply has built-in EMI filter and has over-voltage and over-current protection as well as regulation over line and load variations.

THEORY OF OPERATION

PRIMARY

Power is taken from a 115 volt AC line. A UL approved fusible resistor, R25, limits inrush current as well as acting as a system fuse. The AC current is taken through an EMI filter which suppresses power supply and system noise that would otherwise be reflected back into the power lines.

After the EMI filter, the signal goes to a full-wave bridge rectifier (DB1) then into a capacitive input filter. The combination of these last two items produces a 165 volt DC B+ line from which is run a DC-DC converter.

The DC-DC converter consists of a transistor (Q2) which is used to chop the B+ line at approximately 20 kHz. D2, R9, C8, C9, and D3 are all part of a snubber network designed to protect Q2 as well as suppress ringing which would contribute to line conducted EMI.

SECONDARY

When the power transistor (Q2) is 'ON', energy is stored in the core of the power transformer (T2). The secondary windings are polarized so that the output rectifiers do not conduct while Q2 is ON. When Q2 turns 'OFF', it causes the transformer to 'flyback' which causes the polarity on the output windings of T2 to reverse, allowing the output rectifiers to conduct and deliver energy to the output and output capacitors.

A pi-filter consisting of capacitors on either side of a series filter choke is used to smooth the output waveform, deliver energy during the ON time, and reduce ripple.

FEEDBACK AND CONTROL

On this power supply the only regulated voltage is the +5 volt output. The +12 volt and -12 volt outputs are simply additional secondary windings stacked on top of the +5 volt winding. They track the +5 voltage close enough to provide sufficient regulation to run the circuitry requiring +12 or -12 volts.

The +5 volt output is fed into an error amplifier which compares it to a reference voltage. The output of this amplifier is fed into a control circuit which is magnetically coupled through T1 to the turn-off circuit. This output also controls the ON time of Q2 providing voltage regulation by variations of the duty-cycle.

OVERVOLTAGE PROTECTION

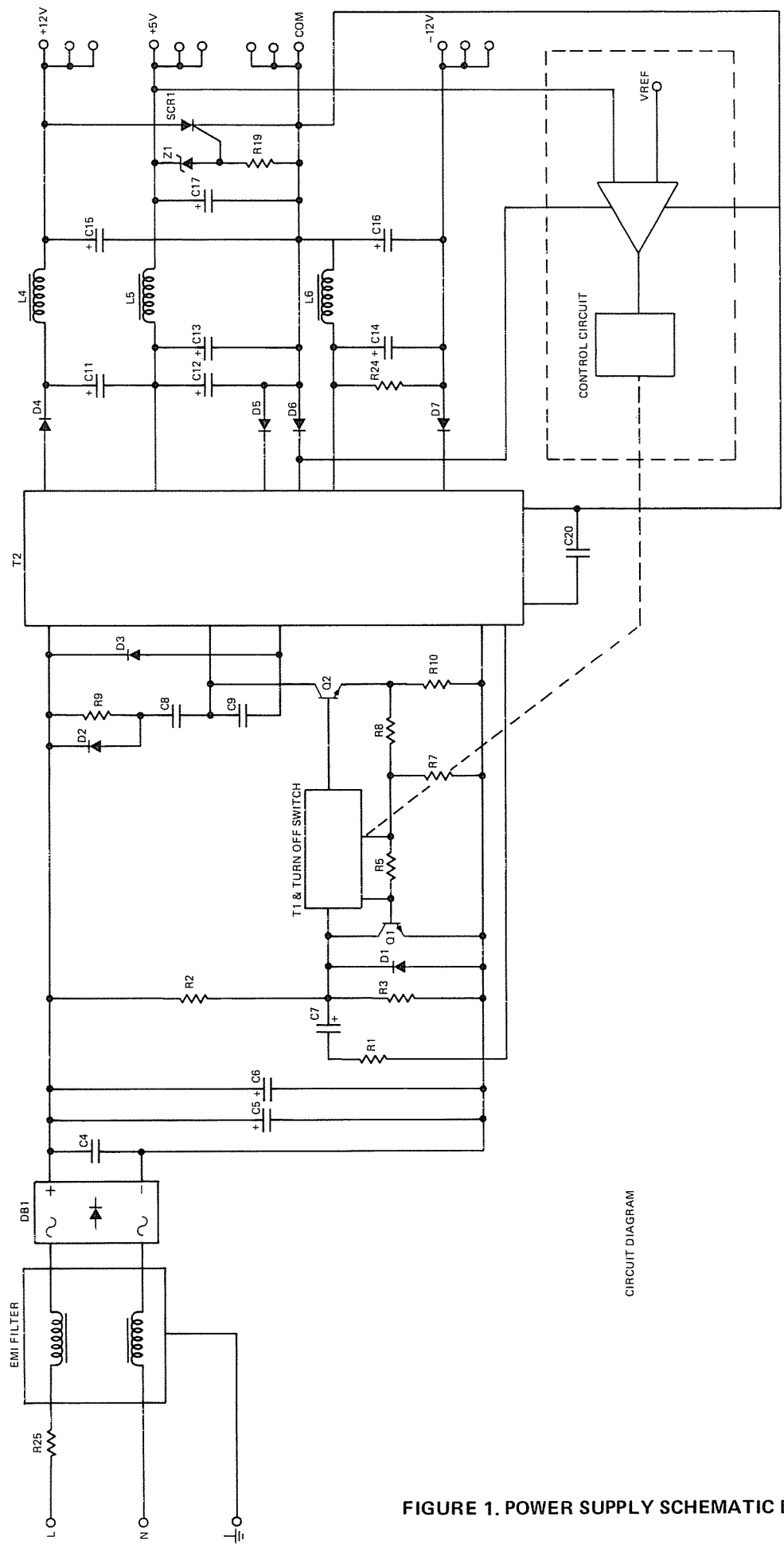
If a failure in the power supply causes the outputs to rise uncontrolled past a specified voltage limit, the power supply will automatically shut down. This is done by sensing the +5 volt output via a Zener diode. When the voltage limit is reached, the SCR is triggered and shorts the +12 volt output to ground. A short on any output will cause the supply to foldback and shut down.

POWER SUPPLY COMPONENT VALUES

SYMBOL

DESCRIPTION

| CAPACITORS | | INTEGRATED CIRCUIT | |
|------------|----------------------------------|--------------------|-----------------------------------|
| C1 | 2200pF, 250VAC, metallized paper | IC1 | Regulator |
| C2 | 0.01μF, 1KV, ceramic | | |
| C3 | 2200pF, 250VAC, metallized paper | | RESISTORS |
| C4 | 0.22μF, 100V, polyester | | |
| C5 | 47μF, 250V, electrolytic | R1 | 47 ohm, 5%, metal oxide film |
| C6 | 100μF, 250V, electrolytic | R2 | 150K, 5%, carbon film |
| C7 | 220μF, 10V, electrolytic | R3 | 1K, 5%, carbon film |
| C8 | 4500pF, 1KV, ceramic | R4 | Not used |
| C9 | 0.01μF, 1KV, ceramic | R5 | 82 ohm, 5%, carbon film |
| C10 | 0.22μF, 100V, polyester | R6 | 27 ohm, 5%, carbon film |
| C11 | 1000μF, 25V, electrolytic | R7 | 3.3 ohm, 5%, carbon film |
| C12 | 1000μF, 25V, electrolytic | R8 | 10 ohm, 5%, carbon film |
| C13 | 1000μF, 25V, electrolytic | R9 | 27 ohm, 5%, metal oxide film |
| C14 | 330μF, 16V, electrolytic | R10 | 75 ohm, 5%, 1W, metal film |
| C15 | 2200μF, 16V, electrolytic | R11 | 270 ohm, 5%, carbon film |
| C16 | 330μF, 16V, electrolytic | R12 | 82 ohm, 5%, carbon film |
| C17 | 470μF, 25V, electrolytic | R13 | 270 ohm, 5%, carbon film |
| C18 | 0.022μF, 50V, polyester | R14 | 8.2 ohm, 5%, carbon film |
| C19 | 0.22μF, 100V, polyester | R15 | 560 ohm, 5%, carbon film |
| C20 | 3900pF, 400VAC, ceramic | R16 | 56 ohm, 5%, carbon film |
| C21 | 0.1μF, 250VAC, metallized | R17 | 56 ohm, 5%, carbon film |
| | | R18 | 12K, 5%, carbon film |
| | | R19 | 12 ohm, 5%, carbon film |
| | | R20 | 470 ohm, 5%, carbon film |
| | | R21 | 2.7K, 2%, metal film |
| | | R22 | 2.7K, 2%, metal film |
| | | R23 | 68K, 5%, carbon film |
| | | R24 | 220 ohm, 5%, 1W, metal oxide film |
| | | R25 | 2 ohm, 5%, fusing metal film |
| | | R26 | 22K, 5%, carbon film |
| | | SCR1 | SCR C122F |
| | | | TRANSFORMERS |
| | | T1 | Control assembly |
| | | T2 | Power assembly |
| | | | TRANSISTORS |
| L1 | Common mode choke assembly | Q1 | PE8050B |
| L2 | Base choke | Q2 | Transistor assembly |
| L3 | 1.5mH, choke | Q3 | PE8550B |
| L4 | Choke coil assembly | | |
| L5 | Choke coil assembly | | |
| L6 | Choke coil | | |



CIRCUIT DIAGRAM

FIGURE 1. POWER SUPPLY SCHEMATIC DIAGRAM

SECTION VII

VIDEO MONITOR

FUNCTIONAL SPECIFICATIONS

The video monitor is a 12-inch solid state monitor designed for display of alphanumeric dot characters. The monitor is designed for a 12-volt DC power input with an average power consumption of 12 watts. The monitor accepts separate video, and vertical drive TTL level inputs.

SPECIFICATIONS

| | |
|-----------------------------|---|
| Cathode Ray Tube: | 12" diagonal, 90° deflection angle, 4 x 5 aspect ratio, P4 phosphor, integral implosion protection. |
| Environment: | Operating Temperature: 41°F to 131°F (5°C to 55°C) ambient Humidity: 95% non-condensing at 41°F to 104°F (5°C to 40°C) Operating Altitude: 10,000 ft. (3046 meters) maximum |
| Power Input: | +12 VDC at 1 amp nominal |
| TTL Level Input Signals: | 4 volts \pm 1.5 volts Horizontal: 4 to 25 μ sec, positive going Vertical: 100 to 1400 μ sec, negative going Video: positive white |
| Video Response: | Bandwidth: 15 MHz, 3 dB Pulse rise time less than 30nsec |
| Scanning Frequency: | Horizontal: 15,600 Hz \pm 500 Hz Vertical: 50/60 Hz |
| Horizontal Retrace: | 10.5 μ sec maximum |
| Vertical Retrace: | 850 μ sec maximum |

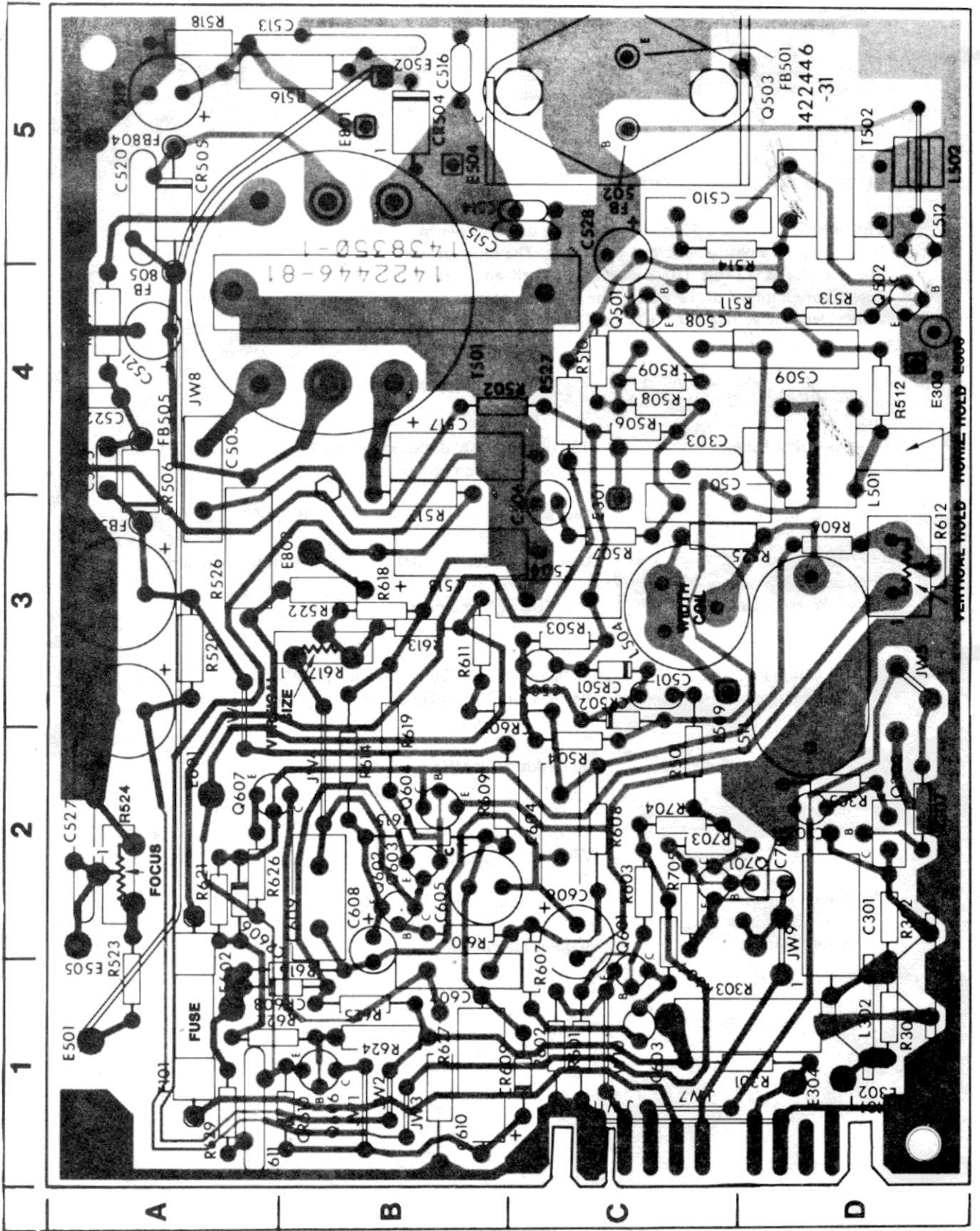


FIGURE 1. VIDEO MONITOR PRINTED CIRCUIT BOARD

SERVICE ADJUSTMENTS

NOTE: Measurements should be made using 12.0 VDC input. Measurements with kine (CRT) attached will require the ground strap from kine be connected to chassis to prevent transistor failures in the event of kine arcing.

FOCUS

Adjust focus control F524 (Figure 1, Zone 2-A) for best overall focus.

VERTICAL SIZE

Adjust vertical size control R617 (Figure 1, Zone 3-B) to produce vertical scan of approximately 6 inches.

HORIZONTAL LINEARITY

Loosen deflection yoke clamp and slide linearity sleeve forward or backward to equalize character spacing on left side of to match character spacing on right side of screen (See Figure 2 for location of linearity sleeve).

WIDTH

Note: Check horizontal linearity prior to width adjustment. Adjust width control to produce horizontal scan of approximately 8 inches.

CENTERING

Adjust centering rings on deflection yoke assembly to center display on screen top to bottom and left to right.

HORIZONTAL HOLD

Horizontal Hold is accomplished by adjustment of the horizontal oscillator coil (Figure 1, Zone 4-D).

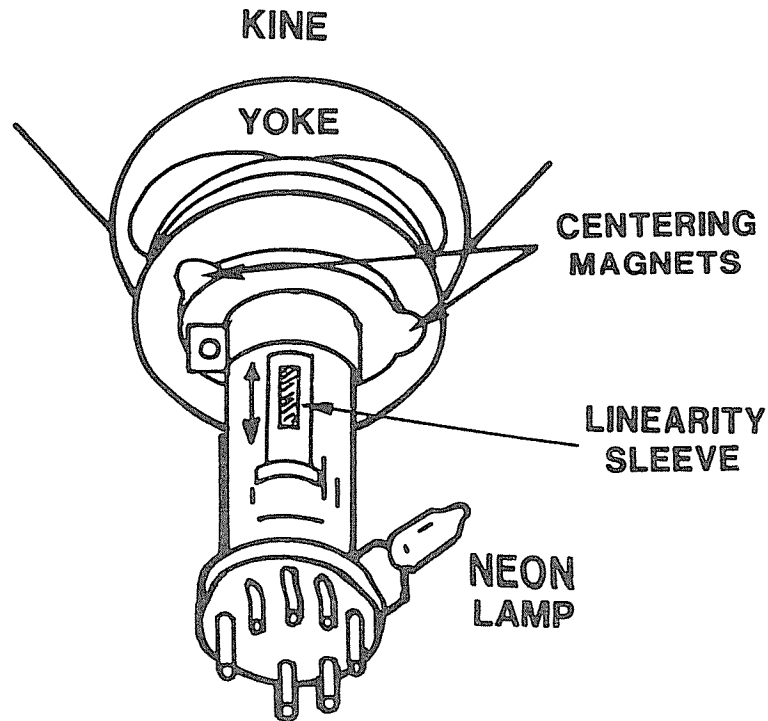
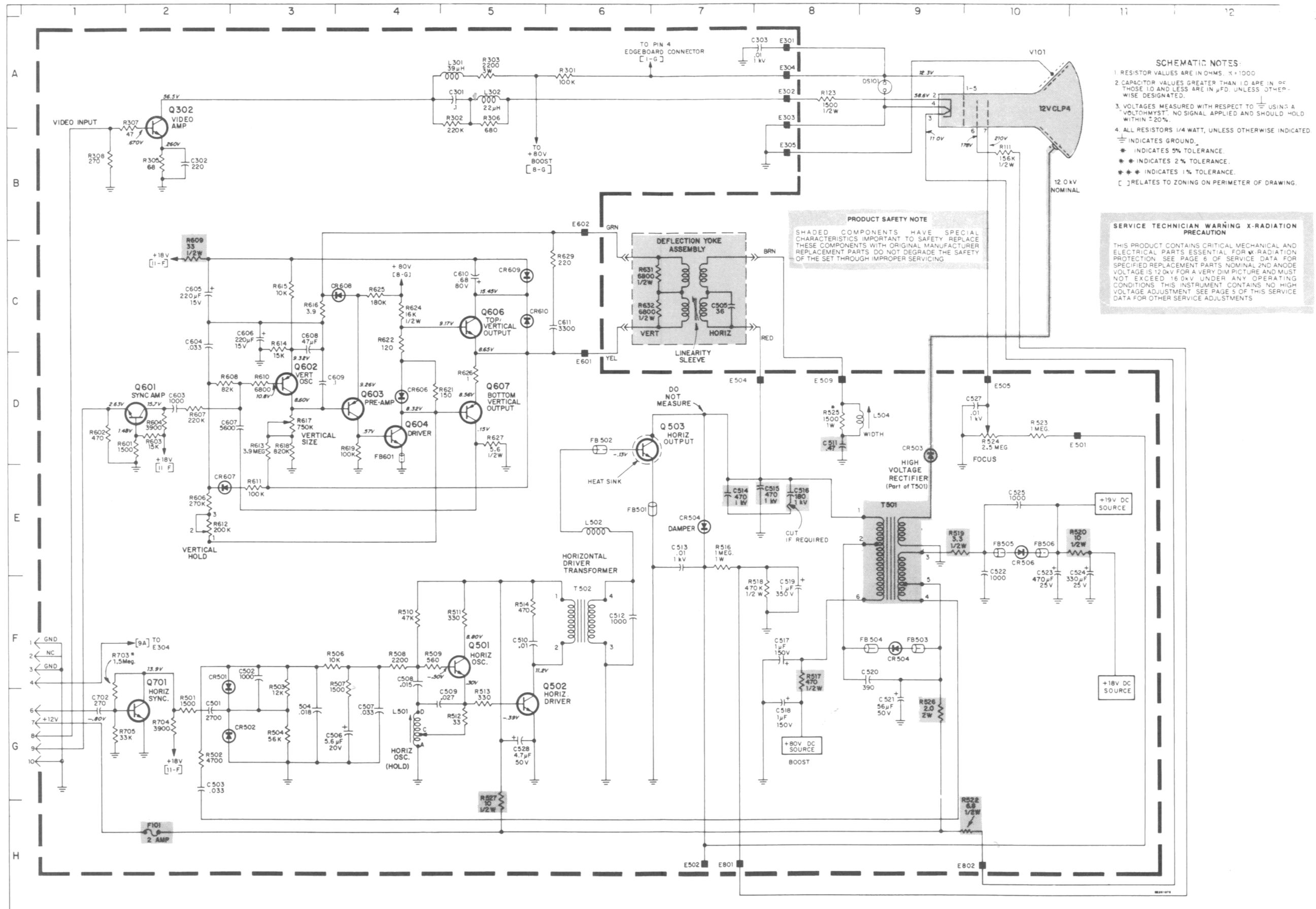


FIGURE 2. DEFLECTION YOKE ASSEMBLY

REPLACEMENT PARTS

PRODUCT SAFETY NOTE—Components marked with a (*) have special characteristics important to safety. Replacement of components marked with a (*) with anything other than the manufacturer's recommended replacement part may result in a safety hazard. Do not degrade the safety of the set through improper servicing or parts replacement.

| SYMBOL NO. | STOCK NO. | DRAWING NO. | DESCRIPTION | SYMBOL NO. | STOCK NO. | DRAWING NO. | DESCRIPTION |
|--------------------------|-----------|-------------|----------------------------|------------|-----------|-------------|---|
| VIDEO MONITOR KIT | | | | | | | |
| | | | KTR-131 | CR609 | 119597 | 1471872-6 | Silicon |
| | | | CHASSIS ASSEMBLY | CR610 | 119597 | 1471872-6 | Silicon |
| | | | VDC-1 | F101 | 148886 | 1479891-6 | * Fuse — 2 amp |
| | | | CAPACITORS | | | | BEADS |
| C301 | 146763 | 1442134-66 | .1 uf 10% 100V film | FB501 | 119971 | 1443391-2 | Ferrite |
| C302 | 147957 | 1491407-12m | 220 pf 10% 50V Z5P disc | FB502 | 119971 | 1443391-2 | Ferrite |
| C303 | 137583 | 945304-125 | .01 uf 20% 1000V disc | FB503 | 119971 | 1443391-2 | Ferrite |
| C501 | 145315 | 1491408-52m | 2700 pf 10% 50V Z5P disc | FB504 | 119971 | 1443391-2 | Ferrite |
| C502 | 143879 | 1491407-91m | 1000 pf 20% 50V Z5P disc | FB505 | 119971 | 1443391-2 | Ferrite |
| C503 | 134778 | 1472442-69 | .033 uf 10% 100V film | FB506 | 119971 | 1443391-2 | Ferrite |
| C504 | 126425 | 1472442-66 | .018 uf 10% 200V film | FB601 | 116761 | 1443391-1 | * Ferrite |
| C505 | 142023 | 942966-224 | 36 pf 5% 500V N750 disc | | | | COILS |
| C506 | 141028 | 1446666-151 | 5.6 uf 20V electrolytic | L301 | 137224 | 973966-54 | 39 uf |
| C507 | 134778 | 1472442-69 | .033 uf 10% 100V film | L302 | 140080 | 973966-65 | 22 uh |
| C508 | 146012 | 1472442-65 | .015 uf 10% 200V film | L501 | 148888 | 1474738-3 | Horiz. hold |
| C509 | 126343 | 1472442-68 | .027 uf 10% 100V film | L502 | 145567 | 1479981-502 | Choke bead |
| C510 | 139441 | 1472442-63 | .01 uf 10% 200V film | L504 | 148887 | 1478648-4 | Width |
| C511 | 138891 | 973991-83 | | | | | TRANSISTORS |
| C512 | 143879 | 1491407-91m | * 1000 pf 20% 50V Z5P disc | Q302 | 141295 | 1417362-3 | Video out |
| C513 | 137583 | 945304-125 | .01 uf 20% 1kV disc | Q501 | 148907 | 1417346-3 | Horizontal oscillator |
| C514 | 425666 | 945304-159 | | Q503 | 140977 | 1417335-1 | Horizontal output |
| C515 | 425666 | 945304-159 | | Q601 | 142711 | 1417306-8 | Vertical integrator |
| C516 | 143029 | 945304-154 | | Q602 | 132830 | 1471112-8 | Vertical oscillator |
| C517 | 146113 | 984655-38 | | Q603 | 132830 | 1471112-8 | Pre amp |
| C518 | 146113 | 984655-38 | 1 uf 150V electrolytic | Q604 | 139268 | 1417318-2 | Vertical driver |
| C519 | 148889 | 1490001-17 | 1 uf 350V electrolytic | Q606 | 141008 | 1417349-2 | Vertical output top |
| C520 | 141002 | 945802-37 | 390 pf 10% 500V N1500 disc | Q607 | 137340 | 1417303-1 | Vertical output bottom |
| C521 | 141285 | 1446667-481 | 56 uf 10% 50V electrolytic | Q701 | 142711 | 1417306-7 | Horizontal sync separator |
| C522 | 120832 | 1420193-63 | 1000 pf 10% 500V disc | | | | RESISTORS |
| C523 | 141432 | 1490306-541 | 470 uf 25V electrolytic | R303 | 149441 | 993260-157 | 2200 ohm 5% 3W ww |
| C524 | 141163 | 1490306-441 | 330 uf 25V electrolytic | R516 | 512510 | 90496-231 | 1 meg ohm 5% 1W |
| C525 | 120832 | 1420193-63 | 1000 pf 10% 500V disc | R517 | 830147 | 993273-389 | * |
| C527 | 137583 | 945304-125 | .01 uf 20% 1kV disc | R519 | 146774 | 993273-337 | * |
| C528 | 142776 | 1490304-561 | 4.7 uf 50V electrolytic | R520 | 830010 | 993273-349 | * |
| C603 | 143879 | 1491407-91m | 1000 pf 20% 50V Z5P disc | R522 | 830A68 | 993273-345 | * |
| C604 | 134778 | 1472442-69 | .033 uf 10% 100V film | R523 | 430227 | 993218-469 | 1 meg ohm 5% 1/4W |
| C605 | 139285 | 1446668-241 | 220 uf 15V electrolytic | R524 | 139062 | 1473359-26 | control focus |
| C606 | 139285 | 1446668-241 | 220 uf 15V electrolytic | R526 | 140983 | 946023-332 | * |
| C607 | 145359 | 1472442-60 | 5600 pf 10% 200V film | R527 | 830010 | 993273-349 | * |
| C608 | 137331 | 1446657-321 | 47 uf 6V electrolytic | R609 | 830033 | 993273-361 | * |
| C609 | 139444 | 1472442-75 | .1 uf 10% 100V film | R612 | 148892 | 1496161-10 | control vertical hold |
| C610 | 145307 | 984655-42 | .68 uf 80V electrolytic | R613 | 148893 | 993218-483 | 3.9 meg ohm 5% 1/4W |
| C611 | 104205 | 1420193-69 | 3300 pf 10% 500V disc | R617 | 149178 | 1473359-47 | control vertical size |
| C702 | 145740 | 1491407-21m | 270 pf 20% 50V Z5P disc | R703 | 147588 | 993218-173 | 1.5 meg ohm 10% 1/4W |
| | | | DIODES | T501 | 148908 | 1465974-505 | * Transformer — high voltage rectifier assembly |
| CR501 | 119597 | 1471872-6 | Horiz AFC | T502 | 146777 | 1479977-3 | Transformer — horizontal driver |
| CR502 | 119597 | 1471872-6 | Horiz AFC | | | | |
| CR504 | 140972 | 1476171-34 | Damper | | 121134 | 1442419-4 | Clamp — yoke |
| CR505 | 140971 | 1476171-33 | +12V run | | 148349 | 1465916-513 | Socket — kine assembly |
| CR506 | 142569 | 1476171-31 | +10V rectifier | | 148894 | 1463734-506 | * Yoke — deflection |
| CR606 | 119597 | 1471872-10 | Silicon | | | | PICTURE TUBE |
| CR607 | 119597 | 1471872-6 | Silicon | | | | 12VCLP4 |
| CR608 | 119597 | 1471872-6 | Silicon | | | | * Picture tube |



- SCHEMATIC NOTES:**
1. RESISTOR VALUES ARE IN OHMS. K = 1000
 2. CAPACITOR VALUES GREATER THAN 10 ARE IN μF . THOSE 10 AND LESS ARE IN μFD . UNLESS OTHERWISE DESIGNATED.
 3. VOLTAGES MEASURED WITH RESPECT TO GND USING A "VOLTOHMYST". NO SIGNAL APPLIED AND SHOULD HOLD WITHIN $\pm 20\%$.
 4. ALL RESISTORS 1/4 WATT, UNLESS OTHERWISE INDICATED.
- ⊥ INDICATES GROUND.
 * INDICATES 5% TOLERANCE.
 ** INDICATES 2% TOLERANCE.
 *** INDICATES 1% TOLERANCE.
 [] RELATES TO ZONING ON PERIMETER OF DRAWING.

PRODUCT SAFETY NOTE

SHADED COMPONENTS HAVE SPECIAL CHARACTERISTICS IMPORTANT TO SAFETY. REPLACE THESE COMPONENTS WITH ORIGINAL MANUFACTURER REPLACEMENT PARTS. DO NOT DEGRADE THE SAFETY OF THE SET THROUGH IMPROPER SERVICING.

SERVICE TECHNICIAN WARNING X-RADIATION PRECAUTION

THIS PRODUCT CONTAINS CRITICAL MECHANICAL AND ELECTRICAL PARTS ESSENTIAL FOR X-RADIATION PROTECTION. SEE PAGE 6 OF SERVICE DATA FOR SPECIFIED REPLACEMENT PARTS. NOMINAL 2ND ANODE VOLTAGE IS 12.0kV FOR A VERY DIM PICTURE AND MUST NOT EXCEED 16.0kV UNDER ANY OPERATING CONDITIONS. THIS INSTRUMENT CONTAINS NO HIGH VOLTAGE ADJUSTMENT. SEE PAGE 5 OF THIS SERVICE DATA FOR OTHER SERVICE ADJUSTMENTS.

FIGURE 3. VIDEO MONITOR ASSEMBLY SCHEMATIC DIAGRAM

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SECTION VIII

ILLUSTRATED PARTS CATALOG

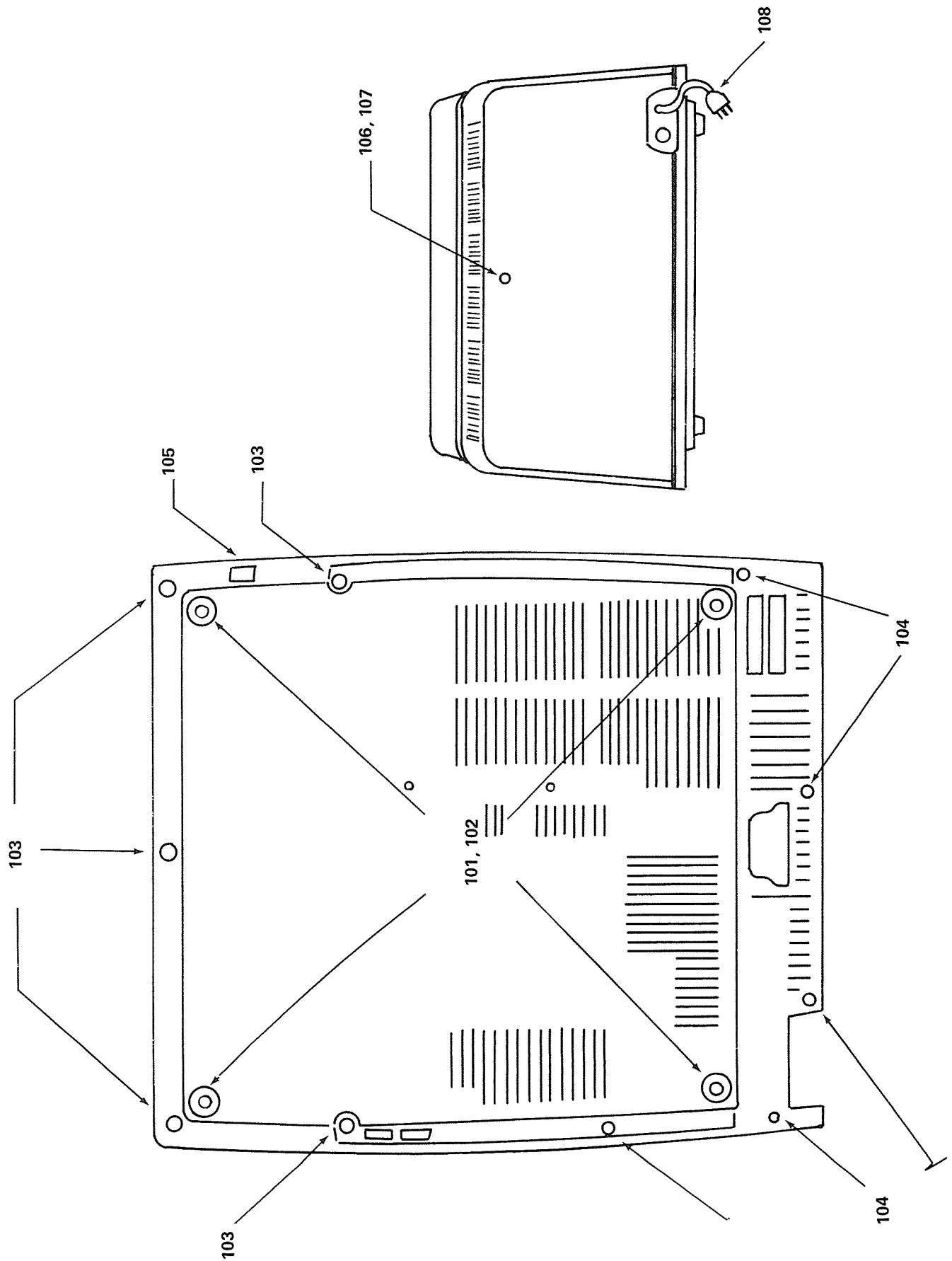


FIGURE 1. OUTER CASE ASSEMBLY

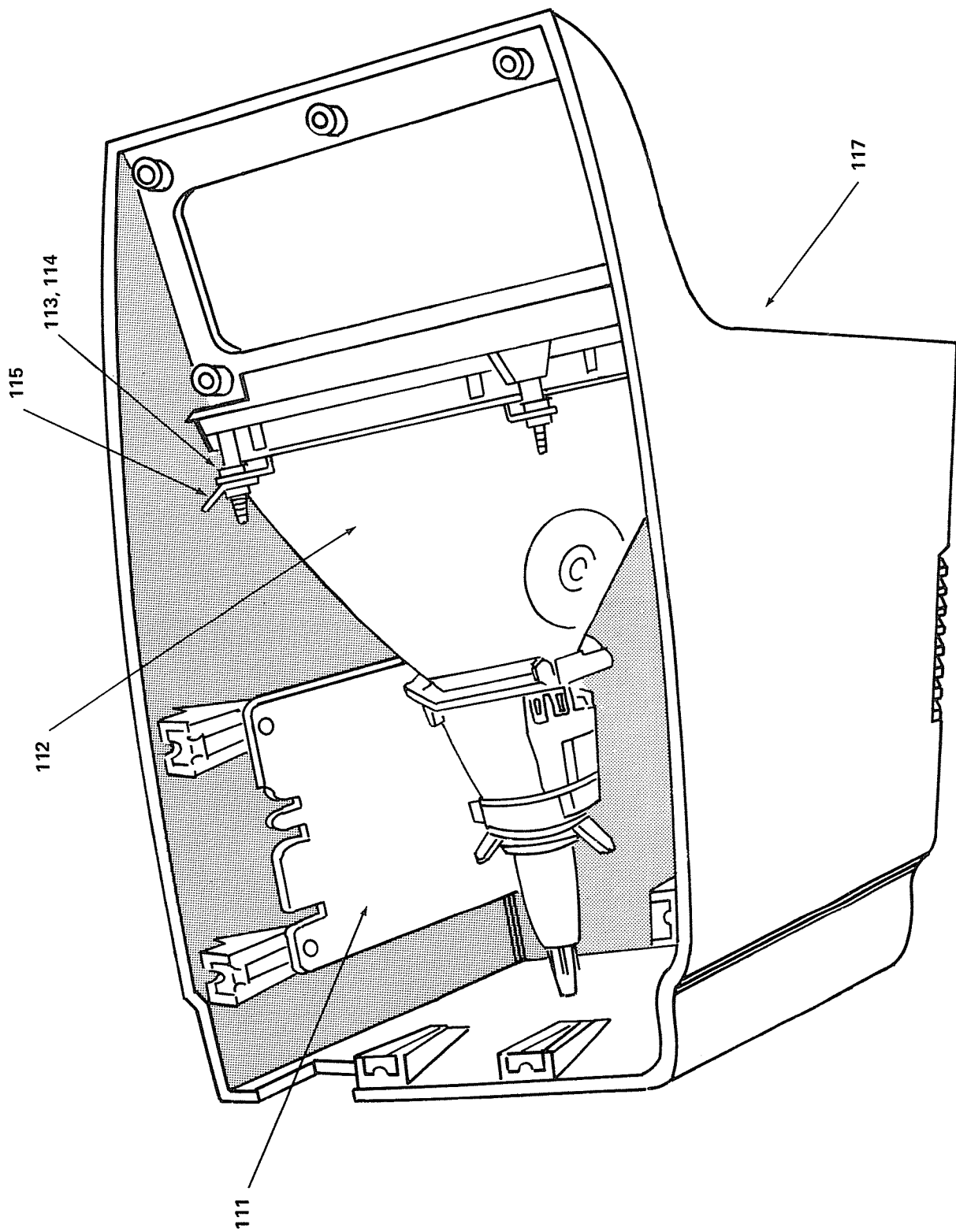


FIGURE 2. CASE TOP ASSEMBLY

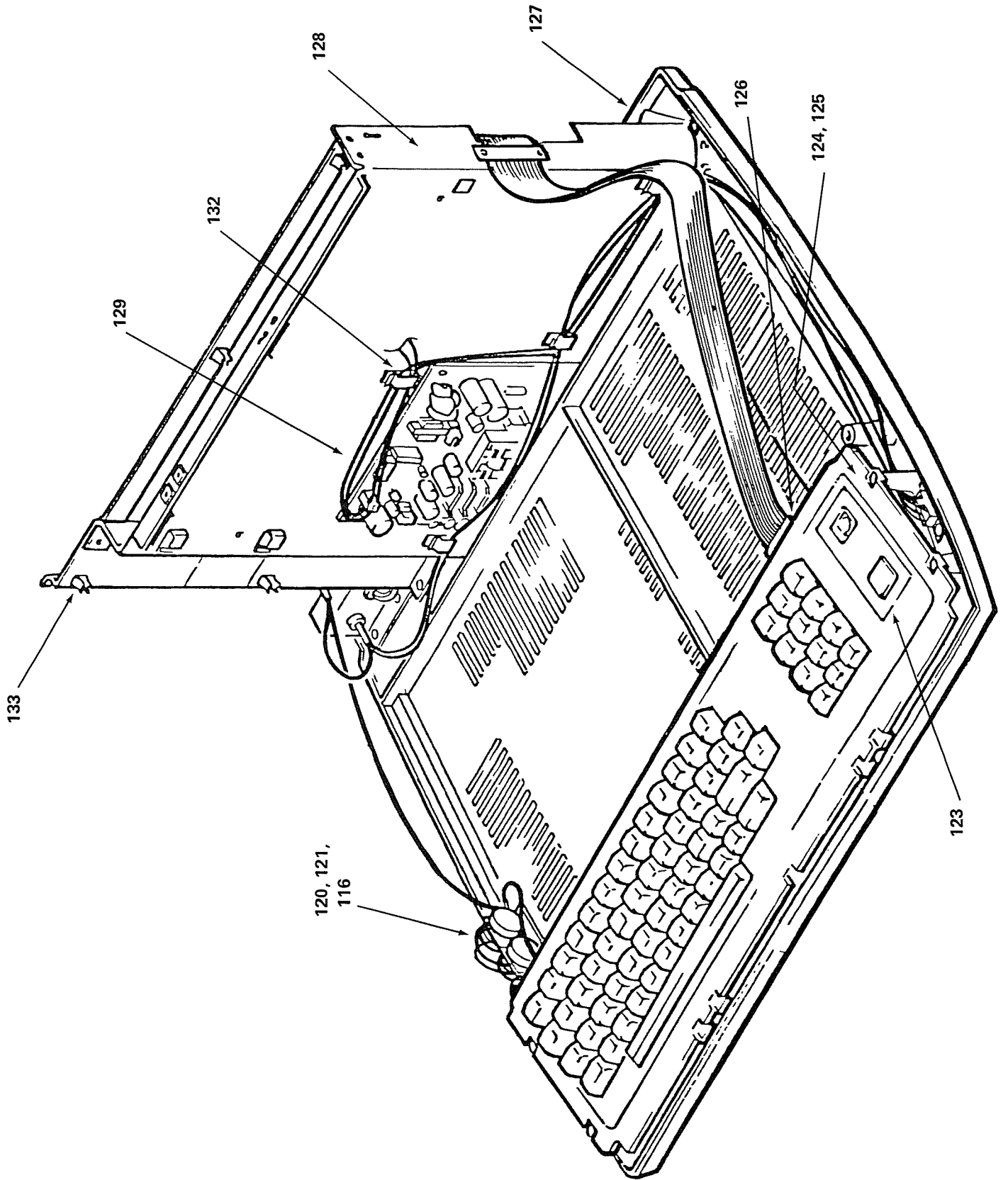


FIGURE 3. BASE PLATE ASSEMBLY

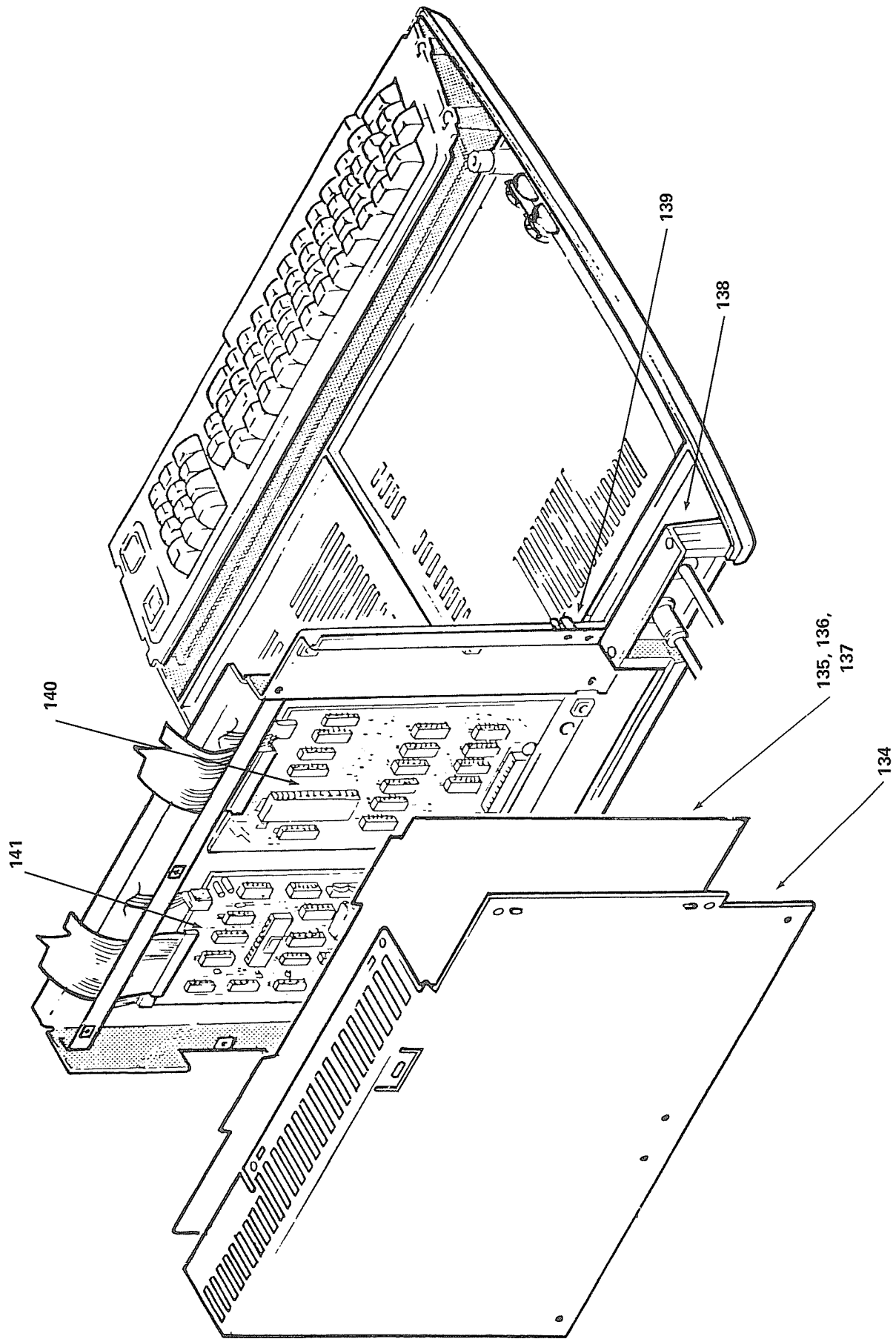


FIGURE 4. METAL CHASSIS ASSEMBLY

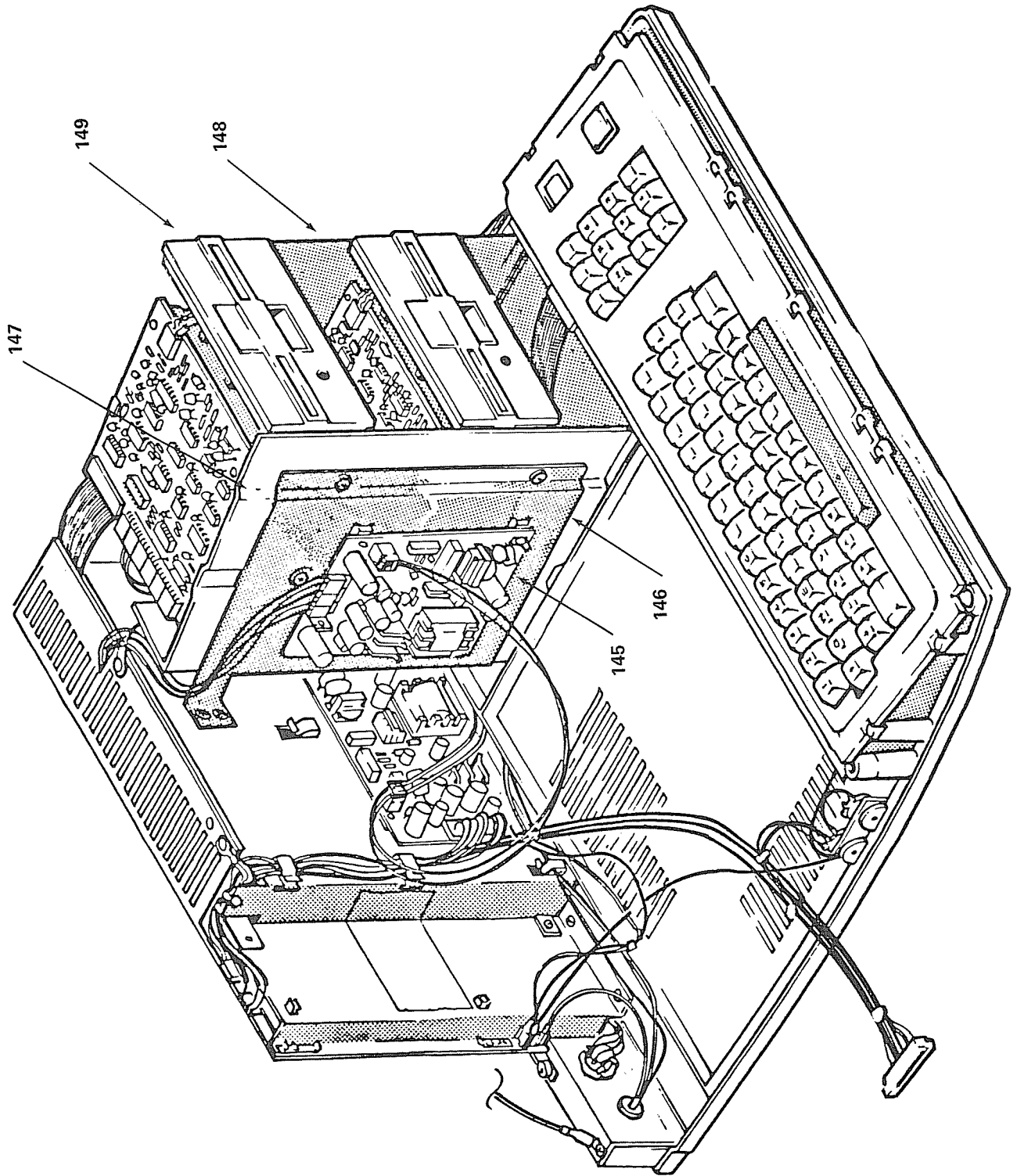


FIGURE 5. DISK DRIVE ASSEMBLY

ILLUSTRATED PARTS CATALOG PARTS LIST

FIGURE 1. OUTER CASE ASSEMBLY

| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|-------------------------------|-------------------------------|----------------------------|
| 101 | Case Feet | 8590098 | AF0297 |
| 102 | Screw, #8 x 3/4", plastite | 8569060 | ----- |
| 103 | Screw, #8 x 1", PH, machine | 8569084 | AHD2308 |
| 104 | Screw, #8 x 3/4", sheet metal | 8569083 | AHD1620 |
| 105 | Power Switch | 8489030 | AS0693 |
| 106 | Screw, #6 x 3/8", sheet metal | 8569088 | AHD1621 |
| 107 | Washer, #6, flat | 8589017 | AHD8514 |
| 108 | Power Cord | 8709138 | AW2540 |

FIGURE 2. CASE TOP ASSEMBLY

| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|----------------------------|-------------------------------|----------------------------|
| 111 | Video Board Assembly | 8492002 | AXX8010 |
| | Screw, #6 x 1/4", plastite | 8569077 | AHD1618 |
| | Shield, mylar | 859014 | ----- |
| 112 | Video Display, CRT | 8492002 | AXX8010 |
| 113 | Washer, #10, flat | 8589038 | AHD8548 |
| 114 | Nut, hex, #10-24 | 8579021 | AHD7180 |
| 115 | Tab, ground, CRT | 8529020 | AHC0329 |
| 117 | Case Top | 8719104 | AZ5689 |

FIGURE 3. BASE PLATE ASSEMBLY

| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|------------------------------|-------------------------------|----------------------------|
| 116 | Screw, #6 x 1/4", plastite | 8569077 | AHD1618 |
| 120 | Knob, Thumbwheel | 8719112 | AK4298 |
| 121 | Video Control Bracket | 8729040 | ART3081 |
| 123 | Label, RAM size, 16K | 8789261 | AHC0321 |
| 124 | Keyboard, 65-key | 8790511 | AXX0205 |
| | Screw, #6 x 1/2", plastite | 8569079 | AHD1619 |
| 125 | Keyboard, Bezel | 8719101 | AZ5688 |
| 126 | Keyboard Header, right angle | 8519107 | AJ6909 |
| *127 | Mylar Shield | 8539015 | ----- |
| 128 | Metal Chassis | Not Stocked | Not Stocked |
| 129 | Power Supply, main | 8790021 | AXX6005 |
| | Fastex, 16404-08 | 8559022 | AHC0075 |
| | Screw, #6 x 3/8" | 8569108 | ----- |
| *132 | Fastex Ground Clip | 8182-67-04 | ----- |
| *133 | Tinnerman clip | 8559029 | AHC0782 |

NOTE: *items may not appear on earlier version units.

**ILLUSTRATED PARTS CATALOG
PARTS LIST (Cont'd)**

FIGURE 4.METAL CHASSIS ASSEMBLY

| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|-----------------------|-------------------------------|----------------------------|
| *134 | Chassis Shield | Not Stocked | Not Stocked |
| 135 | CPU Board Assembly | 8858006 | AXX0507 |
| *136 | Insulating Washers | 8539013 | AHC0787 |
| *137 | Screw, #6 x 5/8", PPH | 8569013 | ----- |
| 138 | Connector Bracket | 8729039 | ART3082 |
| *139 | Ground Bracket | 8729055 | ----- |
| | Screw, #6 x 1/4" | 8569098 | ----- |
| | Washer, #6, star | 8589043 | ----- |
| | Nut, #6 | 8579014 | AHD7168 |
| 140 | RS-232 Board Assembly | ----- | AXX0511 |
| 141 | FDC Board Assembly | 8858029 | AXX0510 |

NOTE: If your computer is earlier the Rev. F, the following hardware may be used on your unit instead of the starred (*) items.

| | | |
|----------------------------|---------|---------|
| PCB Mount Bracket | 729042 | ART3080 |
| Screw, #6 x 1/4", plastite | 8569077 | AHD1618 |
| Clip, RICHCO, LCBS-20R | 8559017 | AHC0070 |
| Fastex, 16404-08 | 8559022 | AHC0075 |
| Clip, RICHCO, LCBS-4R | 8559018 | AHC0071 |
| Fastex, 16402-04 | 8559020 | AHC0073 |

FIGURE 5. DISK DRIVE ASSEMBLY

| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|------------------------------|-------------------------------|----------------------------|
| 145 | Power Supply Disk | 8790021 | AXX6005 |
| 146 | RF Shield | 8729041 | ART3085 |
| 147 | Disk Mounting Bracket, left | 8719106 | ART3083 |
| 148 | Disk Mounting Bracket, right | 8719105 | ART3086 |
| 149 | Disk Drive | 8790112 | AXX5019 |
| 1 | Screw, #6 x 1/4", PPH | 8569077 | ----- |

**ILLUSTRATED PARTS CATALOG
PARTS LIST (Cont'd)**

MISCELLANEOUS

| DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|------------------------------|-------------------------------|----------------------------|
| Cable Clamp | 8729054 | ----- |
| Cable Mount | 8559028 | AHC0358 |
| Cable Tie, 4" | 8559027 | AW2214 |
| Ground Tab, CPU | 8529024 | ----- |
| Ground Tab, Keyboard (0.130) | 8529026 | ----- |
| Ground Tab, Keybaord (0.171) | 8519062 | ----- |

CABLES

| | | |
|--------------------------------|---------|--------|
| AC Power Harness | 8709151 | AW2531 |
| Cassette I/O Internal | 8709156 | AW2538 |
| CRT Wire Harness | 8709153 | AW2356 |
| DC Pwer Harness, Disk | 8709155 | AW2532 |
| DC Power Harness, Main | 8709178 | AW2537 |
| Ground Harness, Disk | 8709204 | ----- |
| Ground Harness, Keyboard | 8709194 | ----- |
| Ground Harness, Main | 8709161 | AW2591 |
| Ground Harness, Secondary Disk | 8709195 | ----- |
| Keyboard/CPU, shielded | 8709182 | ----- |

SECTION IX

MINI DISK DRIVE

SECTION I

GENERAL DESCRIPTION

A. INTRODUCTION

The Disk Drive is a "MINI" Disk Memory designed for random access data entry, storage, and retrieval applications. These applications typically, are intelligent terminal controllers, micro-computers, word processing systems, data communications systems, error logging, micro-program loading and point-of-sale terminals. The Disk Drive is capable of recording and reading digital data using FM, MFM or M²FM techniques.

IMPORTANT NOTICE

A redesigned Logic PC Board has been incorporated into this Manual. Refer to the supplement that follows the Illustrated Parts Catalog section of this book. The supplement contains only the affected paragraphs, illustrations and Parts List.

B. PHYSICAL DESCRIPTION

The electronic components are mounted on two PC Boards: the Logic Board and the Servo Board. There are two versions of the Logic Board, as shown in Figure 2. The Logic Board is located above the chassis, and the Power and Interface signals are connected directly to that Board. The Servo Board (shown in Figure 3) may be mounted in one of two ways, depending on the version of the Servo Board and the type of Disk Drive. The older version, Non-linear Servo Board, is mounted to the rear of the Disk Drive on internal and external units. The newer version, Linear Servo Board, is mounted to the bottom of the Disk Drive on internal units and to the rear of the Drive (the same as the Non-linear Boards) on the external units.

The spindle is belt driven by a DC motor with an integral tachometer. The servo control circuit, pulleys and the tachometer control the speed of the spindle. The read/write/erase head assembly is positioned by means of a stepper motor, split band and a pulley.

C. FUNCTIONAL DESCRIPTION

The Disk Drive is fully self-contained. It consists of a spindle drive system, a head positioning system, and read/write/erase system.

When the front latch is opened, access is provided for the insertion of a 5.25 inch (133.4 mm) standard diskette. The diskette is positioned in place by plastic guides, the front latch and a back stop.

Closing the front latch activates the cone/clamp system which centers and clamps the diskette to the drive hub. The drive hub is driven at a constant speed of 300 rpm by a servo controlled DC motor. In operation, the magnetic head is loaded into contact with the recording medium whenever the front latch is closed.

A 4-phase stepper motor/band assembly and its associated electronics position the magnetic head over the desired track. This positioner employs a one-step rotation to cause a 1-track linear movement. When a write-protected diskette is inserted into the Drive, the write-protect sensor disables the write electronics of the Drive and an appropriate signal is applied to the interface. (When performing a write operation, a 0.013-inch (0.33 mm) [nominal] data track is recorded.)

Data recovery electronics include a low-level read amplifier, differentiator, zero-crossing detector and digitizing circuits. No data decoding facilities are provided in the basic Drive.

The Drive is also supplied with the following sensor systems;

1. A track $\emptyset\emptyset$ switch which senses when the Head/Carriage assembly is positioned at Track $\emptyset\emptyset$.
2. The index sensor (an LED light source and a photo-transistor) is positioned so that when an index hole is detected, a digital signal is generated. The index sensor used is a high resolution device which can distinguish holes placed close together, i.e., index-sector holes in a hard sector diskette.
3. The write-protect sensor disables the Disk Drive electronics whenever a write-protect tab is applied to the diskette.

D. INTERFACE CONNECTIONS

Signal connections for the external Disk Drive are made via a user-supplied 34-pin flat ribbon connector. The internal Drive uses a Radio Shack connector, Part Number AW2535. Both of these connectors mate directly with the PC Board connector (J1) at the rear of the Drive. The DC power connector is a four-pin connector (J2) on the Logic PC Board on the top rear of the Drive.

The signal connector harness should be of the flat ribbon or twisted pair type with the following characteristics:

1. Maximum length of 10 feet (3 M).
2. 22 - 24 gauge conductor compatible with the connector to be used.

Power connections for external Drives should be made with 18 AWG cable. Internal Drives use the Disk DC Power Harness, Radio Shack Part Number AW2532.

| | |
|---|---|
| Media | Industry-compatible 5-1/4 inch (133.4 mm) diskette |
| Tracks per inch | 48 |
| Number of Tracks | 40 |
| Read/Write Track Width | 9.912 inches (252 mm) |
| Dimensions | |
| Height | 3.38 inches (85.85 mm) |
| Width | 5.87 inches (149.10 mm) |
| Depth | 8.0 inches (203.2 mm) |
| Weight | 4.5 lbs (2.04 Kg) |
| Temperature (Exclusive of Media) | |
| Operating | 10°C to 43°C (50°F to 110°F) |
| Non-operating | -40°C to 71°C (-40°F to 160°F) |
| Relative Humidity (Exclusive of Media) | |
| Operating | 20% to 80% |
| Non-operating | 5% to 95% (non-condensing) |
| Vibration | 6 to 600 Hz 0.5g peak |
| Seek Time | 5 msec track to track |
| Head Settling Time | 15 msec (last track addressed) |
| Error Rate | 1 per 10 ⁹ recoverable 1 per 10 ¹² non-recoverable |
| Head Life | 20,000 hours (normal use) |
| Media Life | 3 million passes on a single track |
| Disk Speed | 300 rpm \pm 1.5% (long term) |
| Instantaneous Speed Variation | \pm 3.0% |
| Start/Stop Time | 250 msec (maximum) |
| Transfer Rate | 125/250K bits/sec |
| Bits/Disk (unformatted) | 1.75 million (FM) |
| Recording Modes (typical) | FM, MFM, MMFM |
| Power | +12 V dc \pm 0.6 V, 900 ma maximum 5 V dc \pm 0.25 V, 600 ma maximum |

TABLE 1. MINI-DISK DRIVE MECHANICAL AND ELECTRICAL SPECIFICATIONS.

E. PHYSICAL CHECKOUT

Before applying power to the unit, the following inspection should be performed:

1. Front latch. Check that the front latch opens and closes. Note that when the door is opened, the head arm raises.
2. Ensure that the front panel is secure.
3. Manually rotate the drive hub. The hub should rotate freely.
4. Check that the PC boards are secure. Check that the connectors are firmly seated. Also, check the location of the Servo Board for type (Linear or Non-linear).

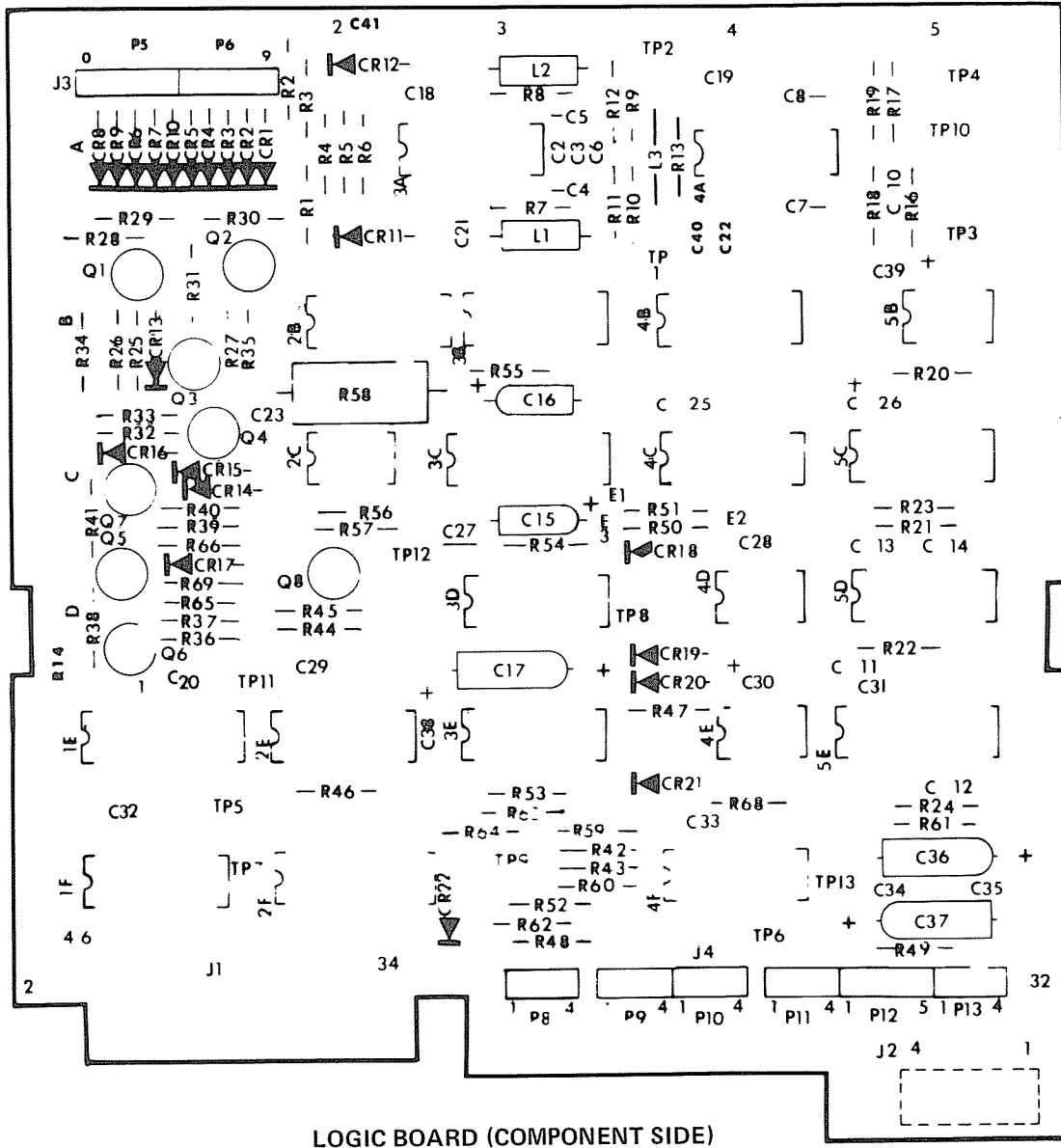


FIGURE 1. LOGIC PC BOARD COMPONENT LOCATIONS

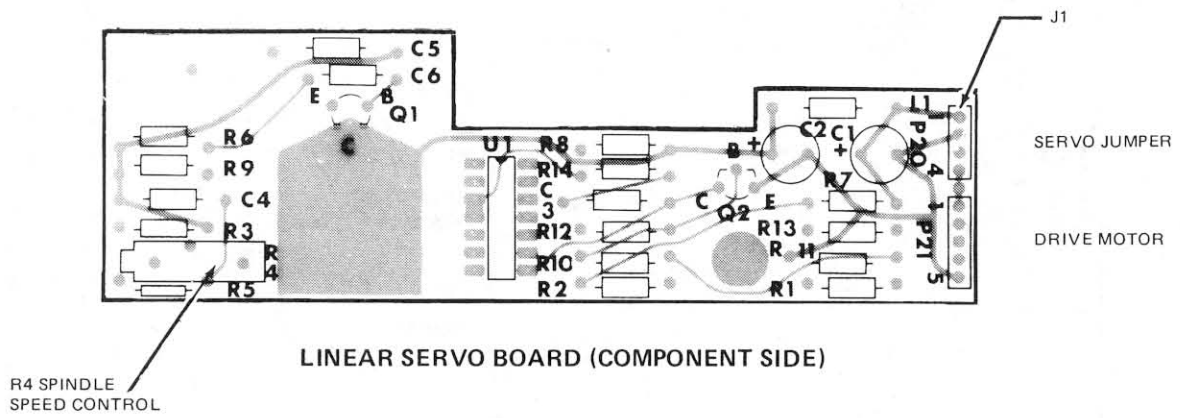
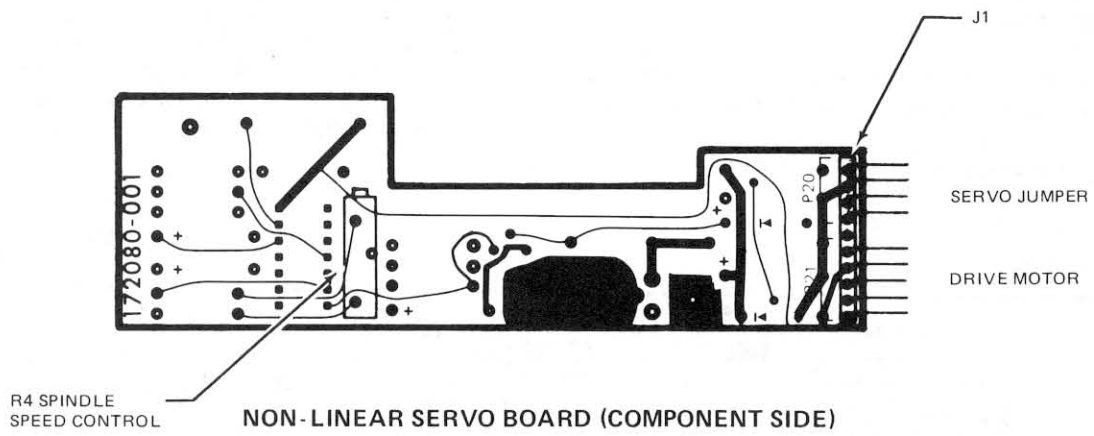


FIGURE 2. SERVO PC BOARD COMPONENT LOCATIONS

5. Check for debris or foreign material between the heads and remove same.

6. Check plastics for broken or cracked pieces, e.g., write protect lever, guide rails, etc.

NOTE: To ensure proper operation of the Drive, the chassis should be connected to earth ground. The 3/16-inch (4.76 mm) male QC lug, located at the rear of the chassis, is provided for this connection.

F. MOUNTING THE DISK DRIVE

The Drive can be mounted in any plane, i.e., upright, horizontal or vertical. However, when it is mounted horizontally, the Logic PC board side of the chassis must be the uppermost side. Tapped holes are provided in various locations for the attachment of user-supplied hardware.

G. RESISTOR TERMINATION

(See Figure 3)

1. The Resistor Termination in IC socket (2F) is used only in the last Drive in the system. It must be removed for Drive 2 when two external drives are used.

NOTE: The internal Drives in the Model III Computer are not terminated.

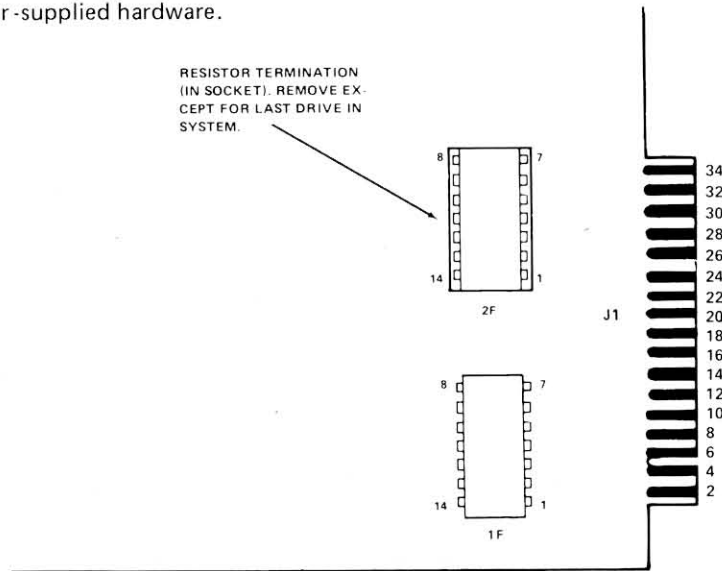


FIGURE 3. RESISTOR TERMINATION

H. FLAT RIBBON CABLE ASSEMBLY

(See Figure 4)

Pins must be removed from Drive connectors on the Cable Assembly as follows and as illustrated:

1. Connector for the first internal drive (Drive 0) and the first external drive (Drive 2) pins 12, 14 and 32.

2. Connector for the second internal drive (Drive 1) and the second external drive (Drive 3), pins 10, 14 and 32.

| INTERNAL DRIVES | | EXTERNAL DRIVES | |
|-------------------|------------------|------------------|--------------------|
| DRIVE NUMBER ZERO | DRIVE NUMBER ONE | DRIVE NUMBER TWO | DRIVE NUMBER THREE |
| 12 | 10 | 12 | 10 |
| 14 | 14 | 14 | 14 |
| 32 | 32 | 32 | 32 |

FIGURE 4. CABLE ASSEMBLY – CONNECTOR PIN REMOVAL CHART

SECTION II

THEORY OF OPERATION

A. INTRODUCTION

The Disk Drive consists of the mechanical and electrical components necessary to record and read digital data on a diskette. DC power at $\pm 12V$ and $+5V$ (provided by the user for the external drives) is required for operation.

B. ORGANIZATION OF THE DISK DRIVE

All electrical subassemblies in the Disk Drive are constructed with leads which terminate in 4 or 5 pin connectors, enabling the individual assemblies to be removed.

The magnetic head is connected to the PC board via a cable terminating in a 5-pin female connector and its associated male socket which is located in close proximity to the read/write data electronics.

Interface signals and power are provided via connectors at the rear of the Drive. A detailed description of these signals is presented in Section III of this manual.

C. FUNCTIONAL BLOCK DIAGRAM DESCRIPTION

Figure 5 is a functional block diagram of the Disk Drive and should be referred to in conjunction with the following discussion:

The Disk Drive consists of the following functional groups:

- ★ Index Pulse Shaper
- ★ Write Protect Sensor
- ★ Track 00 Sensor
- ★ Spindle Drive Control
- ★ Carriage Position Control
- ★ Write/Erase Control
- ★ Read Amplifier and Digitizer

D. INDEX

An index pulse is provided to the user system via the INDEX PULSE interface line. The index circuitry consists of an Index LED, Index Phototransistor and a Pulse Shaping Network. As the index hole in the disk passes the Index LED/Phototransistor combination, light from the LED

strikes the Index Phototransistor causing it to conduct. The signal from the Index Phototransistor is passed to the Pulse Shaping Network which produces a pulse for each hole detected. This pulse is presented to the user on the INDEX PULSE interface line.

E. WRITE PROTECT

A Write Protect signal is provided to the user system via the WRITE PROTECT interface line. The write protect circuitry consists of a Write Protect Sensor and circuitry to route the signal produced.

When a write protected diskette is inserted in the drive, the sensor is activated and the logic disables the write electronics and supplies the status signal to the Interface.

F. TRACK 00 SWITCH

The level on the TRACK 00 interface line is a function of the position of the magnetic head assembly. When the head is positioned at Track 00 and the stepper motor is at the home position, a true level is generated and sent to the user.

G. SPINDLE DRIVE

The Spindle Drive system consists of a spindle assembly driven by a DC motor-tachometer combination through a drive belt.

Associated with the spindle drive motor are the servo electronics required for control.

The control circuitry also includes a current limiter and an interface control line. When the DRIVE MOTOR ENABLE interface line is true, the drive motor is allowed to come up to speed. When the current through the drive motor exceeds 1.3 A, the current limit circuitry disables the motor drive.

H. POSITIONER CONTROL

The Head Positioning system utilizes a four-phase stepper motor drive which changes one phase for each track advancement of the Read/Write carriage. In addition to the logic necessary for motion control, a gate is provided as an element for inhibiting positioner motion during a write operation.

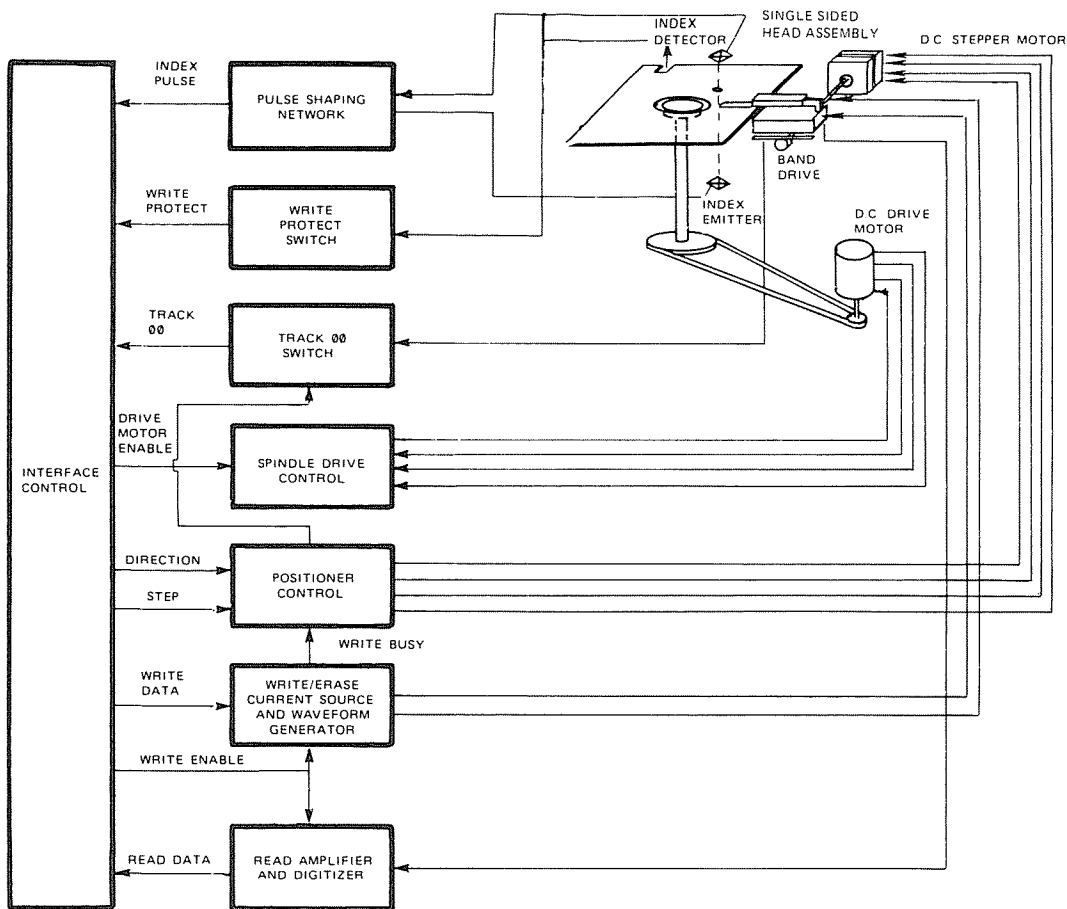


FIGURE 5. FUNCTIONAL BLOCK DIAGRAM

I. DATA ELECTRONICS

Information can be recorded on the diskette using a double-frequency code. Figure 6 illustrates the magnetization profiles in each bit cell for the number sequence shown.

The erase gaps provide an erased guard band on either side of the recorded track. This accommodates the tolerances in track positioning.

All signals required to control the data electronics are provided by the user system and are shown in the Block Diagram (Figure 5). These control signals are:

- ★ SELECT
- ★ WRITE ENABLE
- ★ WRITE DATA

The READ DATA composite signal is sent to the user system via the interface.

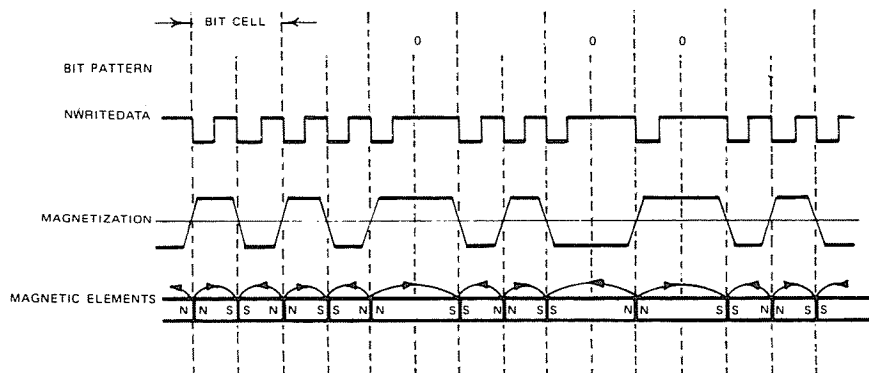


FIGURE 6. FM RECORDING

J. DATA RECORDING

Referring to Figure 5, it can be seen that the Write Electronics consists of a Write/Erase Current Source and Write Waveform Generator, Erase Current Source, and Trim Erase Control Logic.

The read/write winding on the magnetic head is center-tapped. During a write operation, current from the Write Current Source flows in alternate halves of the winding under control of the Write Waveform Generator.

Before recording can begin, certain conditions must be satisfied. The conditions required for recording (i.e., unit ready) must be established by the user system as follows:

- (1) Drive speed stabilization. This condition will exist 250 mSec after starting the drive motor.
- (2) Subsequent to any step operation, the positioner must be allowed to settle. This requires 20 mSec total after the last step pulse is initiated, i.e., 5 mSec for the step motion and 15 mSec for settling.

NOTE: All of the foregoing operations can be overlapped, if required.

Figure 7 shows the relevant timing diagram for a write operation. At $t = 0$ when the unit is ready, the WRITE ENABLE interface line goes true; this enables the Write Current source.

Since the trim erase gaps are behind the read/write gap, TRIM ERASE control goes true 390 μ Sec after the WRITE ENABLE interface line. It should be noted that this value is optimized between the requirements at Track 00 and Track 40 so that the effect of the trim erase gaps on previous information is minimized.

Figure 7 also shows the information on the WRITE DATA interface line and the output of the Write Waveform Generator which toggles on the leading edge of every WRITE DATA pulse.

Note that a minimum of 4 μ Sec and a maximum of 8 μ Sec between WRITE ENABLE going true and the first WRITE DATA pulse is only required if faithful reproduction of the first WRITE DATA transition is significant.

At the end of recording, at least one additional pulse on the WRITE DATA line must be inserted after the last significant WRITE DATA pulse to avoid excessive peak shift effects.

The TRIM ERASE signal must remain true for 800 μ Sec after the termination of WRITE ENABLE to ensure that all recorded data are trim erased. This value is again optimized between the requirements at Tracks 00 and 40.

The duration of a write operation is from the true-going edge of WRITE ENABLE to the false-going edge of TRIM ERASE. This is indicated by the internal WRITE BUSY waveform shown.

K. DATA REPRODUCTION

The Read Electronics consists of the following:

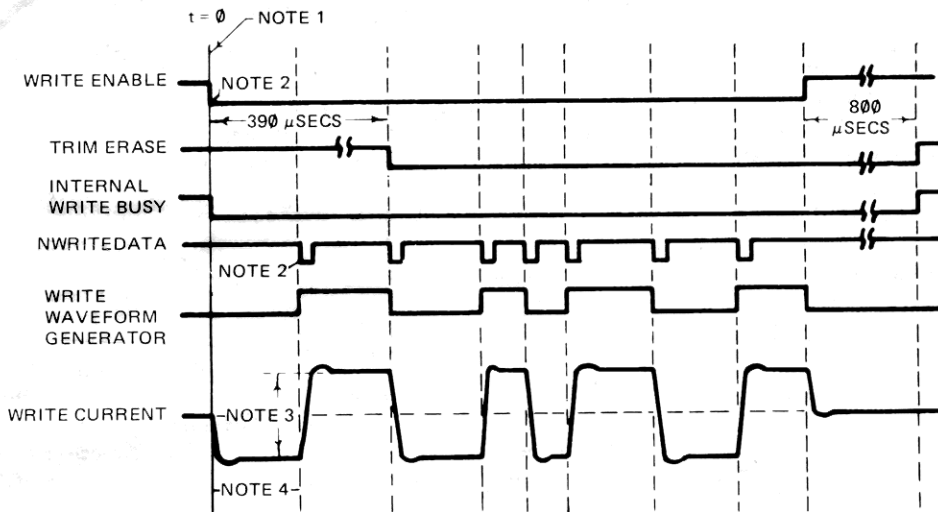
- ★ Read Switch
- ★ Read Amplifier
- ★ Filter
- ★ Differentiator
- ★ Comparator and Digitizer

The Read Switch is used to isolate the Read Amplifier from electrical signals across the magnetic head during a write operation.

Before reading can begin, the Drive must be in a ready condition. As with the data recording operation, this ready condition must be established by the user system. In addition to the requirements established in the paragraph, DATA RECORDING, a 100 μ Sec delay must exist from the trailing edge of the TRIM ERASE signal to allow the Read Amplifier to settle after the transient caused by the Read Switch returning to the Read mode.

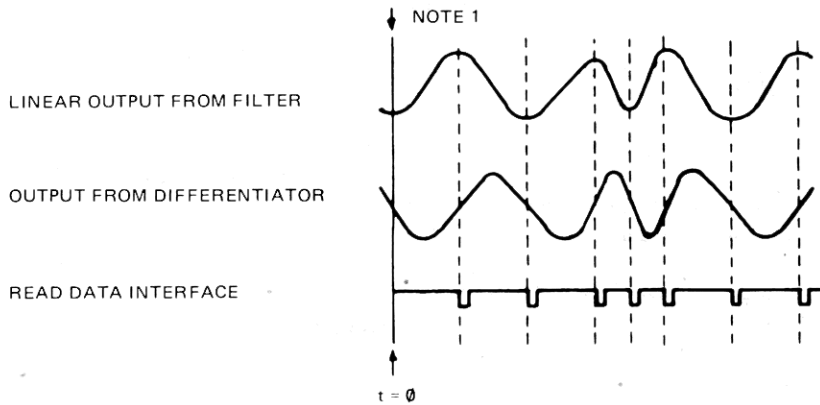
Referring to Figure 8, the output signal from the read/write head is amplified by a read amplifier and filtered to remove noise by a Linear Phase Filter. The linear output from the Filter is passed to the Differentiator which generates a waveform whose zero crossovers correspond to the peaks of the read signal. This signal is then fed to the Comparator and Digitizer circuit.

The Comparator and Digitizer circuitry generates a 1 μ Sec READ DATA pulse corresponding to each peak of the read signal. This Composite Read Data signal is then sent to the user system via the READ DATA interface line.



- NOTES:
- | | |
|---|--|
| <p>1. $t = 0 = 250$ MILLISECONDS AFTER DRIVE MOTOR STARTS, OR 20 MILLISECONDS AFTER LAST STEP PULSE (WHICHEVER IS THE LATEST TIME).</p> | <p>2. UNSYNCHRONIZED</p> <p>3. 8.5 MA PEAK TO PEAK</p> <p>4. 4 μSECONDS MINIMUM. 8 μSECONDS MAXIMUM</p> |
|---|--|

FIGURE 7. WRITE TIMING DIAGRAM



- NOTES:
- $t = 0 = 250$ MILLISECONDS AFTER DRIVE MOTOR STARTS, OR 20 MILLISECONDS AFTER STEP COMMAND, OR 100 μSECONDS AFTER TERMINATION OF WRITE BUSY (WHICHEVER IS THE LATEST TIME)

FIGURE 8. READ TIMING DIAGRAM

SECTION III OPERATION

A. INTRODUCTION

This section contains the interface description and the electrical adjustments necessary for the Disk Drive.

B. INTERFACE ELECTRONICS SPECIFICATIONS

All interface signals are TTL compatible. Logic true (low) is +0.4 V (maximum). Logic false (high) is +2.4 V (minimum). Figure 9 illustrates the interface configuration.

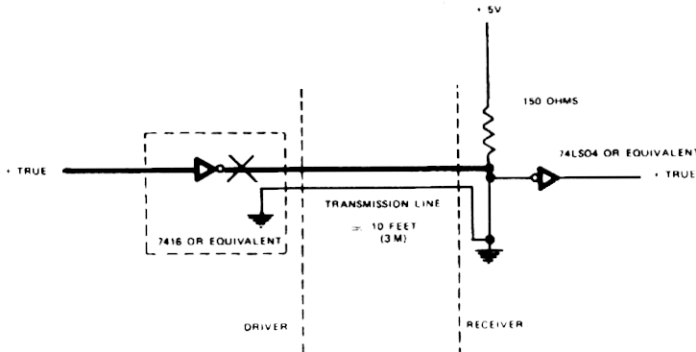


FIGURE 9. INTERFACE CONFIGURATION

It is recommended that the interface cable be a flat ribbon cable, with a characteristic impedance of 100 ohms. (or equivalent twisted pairs). Maximum interface cable length is 10 feet (3 M).

Interface connector pin assignments and power connector pin assignments are given in Table 2 and Table 3.

C. INPUT CONTROL LINES (See Table 2)

D. SELECT LINES (DS1* - DS4*)

The SELECT lines provide a means of selecting and deselecting a Disk Drive. These four lines (DS1* - DS4*) select one of the four Disk Drives attached to the controller. When the signal logic level is true (low), the Disk Drive electronics are activated and the Drive is conditioned to respond to step or read/write commands. When the logic level is false (high) the input control lines and output status lines are disabled.

A SELECT line must remain stable in the true (low) state until the execution of a step or read/write command is completed.

The Disk Drive address is determined by SELECT lines 1 through 4 (or a DIP Shunt in the 1E position) on the PC board. These lines provide a means of daisy-chaining a maximum of four Disk Drives to a controller. Only one line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more SELECT lines are in the true (low) state simultaneously.

E. DRIVE MOTOR ENABLE (MOTORON)

When this signal line logic level goes true (low), the drive motor accelerates to its nominal speed of 300 rpm and stabilizes in less than 250 mSec. When the logic level goes false (high), the Disk Drive decelerates to a stop.

F. DIRECTION AND STEP (DIR*) (STEP*)

When the Disk Drive is selected, a true (low) pulse with a time duration greater than 200 nSec on the STEP line initiates the access motion. The direction of motion is determined by the logic state of the DIRECTION line when a STEP pulse is issued. The motion is towards the center of the disk if the DIRECTION line is in the true (low) state when a STEP pulse is issued. The direction of motion is away from the center of the disk if the DIRECTION line is in the false (high) state when a STEP pulse is issued. To ensure proper positioning, the DIRECTION line should be stable 0.1 μ Sec (minimum) before the trailing edge of the corresponding STEP pulse and remain stable until 0.1 μ Sec after the trailing edge of the STEP pulse. The access motion is initiated on the trailing edge of the STEP pulse.

G. COMPENSATED WRITE DATA (CWD)

When the Disk Drive is selected, this interface line provides the bit-serial WRITE DATA pulses that control the switching of the write current in the head. The write electronics must be conditioned for writing by the WRITE ENABLE line (refer to the WRITE ENABLE paragraph below).

For each high-to-low transition on the WRITE DATA line, a flux change is produced at the head write gap. This causes a flux change to be stored on the disk.

When the double-frequency type encoding technique is used (in which data and clock form the combined Write Data signal), it is recommended that; when writing all zeroes, the repetition rate of the high-to-low transitions be equal to the nominal data rate, $\pm 0.1\%$. The repetition rate of the high-to-low transitions, when writing all ones, should be equal to twice the nominal data rate, $\pm 0.1\%$.

H. WRITE GATE (WG*)

When this signal is true (low), the write electronics are prepared for writing data (read electronics disabled). This signal turns on write current in the read/write head. Data is written under control of the WRITE DATA input line. It is generally recommended that changes of state on the WRITE ENABLE line occur before the first WRITE DATA pulse. However, the separation between the leading edge of WRITE ENABLE and the first significant WRITE DATA pulse should not be less than 4 μ Sec and not greater than 8 μ Sec. The same restrictions exist for the relationship between the least significant WRITE DATA pulse and the

| Controller-to-Disk Drive | | |
|--------------------------|--------|-------------------------------|
| Ground | Signal | Description (Mnemonic) |
| 1 | 2 | Connector clamp |
| 3 | 4 | (Spare) |
| 5 | 6 | (Spare) |
| 9 | 10 | SELECT 1 (NDS1) |
| 11 | 12 | SELECT 2 (NDS2) |
| 13 | 14 | SELECT 3 (NDS3) |
| 15 | 16 | DRIVE-MOTOR ENABLE (NMOTORON) |
| 17 | 18 | DIRECTION |
| 19 | 20 | STEP (NSTEP) |
| 21 | 22 | WRITE DATA (NWRITEDATA) |
| 23 | 24 | WRITE GATE (NWRITEGATE) |
| 31 | 32 | SELECT 4 (NDS4) |

| Disk Drive-to-Controller | | |
|--------------------------|--------|-------------------------------|
| Ground | Signal | Description (Mnemonic) |
| 7 | 8 | INDEX (NINDEX/SECTOR) |
| 25 | 26 | TRACK 00 (NTRK00) |
| 27 | 28 | WRITE PROTECT (NWRITEPROTECT) |
| 29 | 30 | READ DATA (NREADDATA) |
| 33 | 34 | Connector Clamp |

**TABLE 2. DISK DRIVE EDGE CARD PIN ASSIGNMENTS – J1.
(J2 on the Redesigned Logic/Servo P C Board)**

| Pin | Supply Voltage |
|-----|-------------------|
| 1 | +12 V DC |
| 2 | Return (+12 V DC) |
| 3 | Return (+5 V DC) |
| 4 | +5 V DC |

**TABLE 3. POWER CONNECTOR
PIN ASSIGNMENTS**

termination of the WRITE ENABLE signal. When the WRITE ENABLE line is false (high), all write electronics are disabled.

When a write protected diskette is installed in a Disk Drive, the write electronics are disabled irrespective of the state of the WRITE ENABLE line.

I. OUTPUT STATUS

(See Table 2)

J. INDEX PULSE (IP*)

The INDEX PULSE signal is provided once each revolution (200 mSec, nominal) to indicate to the controller the beginning of a track. The INDEX PULSE line remains in the true (low) state for the duration of the INDEX PULSE (The duration of an INDEX PULSE is nominally 4.0 mSec).

The leading edge of an INDEX PULSE must always be used to ensure diskette interchangeability between Disk Drives.

K. TRACK 00 (TRK0*)

When the Disk Drive is selected, the TRACK 00 interface signal indicates to the controller that the read/write head is positioned at Track 00. The Track 00 remains true (low) until the head is moved away from Track 00.

L. WRITE PROTECT (WPRT*)

When the Disk Drive is selected, this signal line logic level goes true (low) when the diskette is write protected. The write electronics are internally disabled when the diskette is write protected.

NOTE: It is recommended that the write data line be inactive whenever Write Enable is false (i.e., read state).

When the level on this line is false (high), the write electronics are enabled and the write operation can be performed. It is recommended that the controller not issue a write command when the WRITE PROTECT signal is true (low).

M. READ DATA (RD*)

This interface line transmits the readback data to the controller when the Drive is selected. It provides a pulse for each flux transition recorded on the medium. The READ DATA output line goes true (low) for a duration of 1 μ Sec for each flux change recorded.

The leading edge of the READ DATA output pulse represents the true positions for the flux transitions on the diskette surface.

SECTION IV

MAINTENANCE

A. PHYSICAL DESCRIPTION OF THE PC BOARD

The Logic PC board is approximately 6 inches (152 mm) long by 5.5 inches (139 mm) wide. Figure 10 illustrates the placement of test points and connectors.

B. CIRCUIT BOARD TEST POINTS

The following test point description assumes that the Logic and Servo P.C. boards are installed in the Drive and that the Drive is in an operational mode with a diskette installed:

Logic Ground (TP6)

Digital Logic ground is referenced at TP6.

Differentiated Read Signal (TP3, TP4)

These test points are provided to observe the differential output of the second stage amplifier and differentiated read signal.

Read Data Single Shot (TP5)

The output of the single shot used in the read section is nominally 1.0 μ sec for each flux transition detected.

Index Pulse (TP7)

With a standard soft sectored diskette installed, the signal is a high going pulse, nominally 4.0 msec in duration every 200 msec.

Amplified Read Signal (TP1, TP2)

These test points are provided to observe the differential output of the first stage of read signal amplification.

Motor On (TP13)

This signal is low true for the "motor on" condition.

Track 00 (TP8)

This signal is low true when the carriage is positioned at track 00 and the step motor phase is correct.

Analog Ground (TP10)

The analog ground reference point is provided for measuring read/write waveforms.

Step Pulse (TP12)

When stepping in or out, the signal is a high going pulse for each step of the carriage.

Write Protect Switch (TP9)

When a write protected diskette is installed in the Drive, the signal is high.

C. OPTION SELECT

Input Line Terminations

The Disk Drive has been provided with the capability of terminating the input lines listed below:

- ★ Motor On
- ★ Direction Select
- ★ Step
- ★ Write Data
- ★ Write Gate

These lines are terminated through a 150 ohm resistor pack installed in a DIP socket located at IC location 2F.

In a multiple drive system, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. Catalog Numbers 26-1160 and 26-1164 are shipped with the termination resistor installed. Catalog Numbers 26-1161/1162/1163 are shipped without a resistor pack.

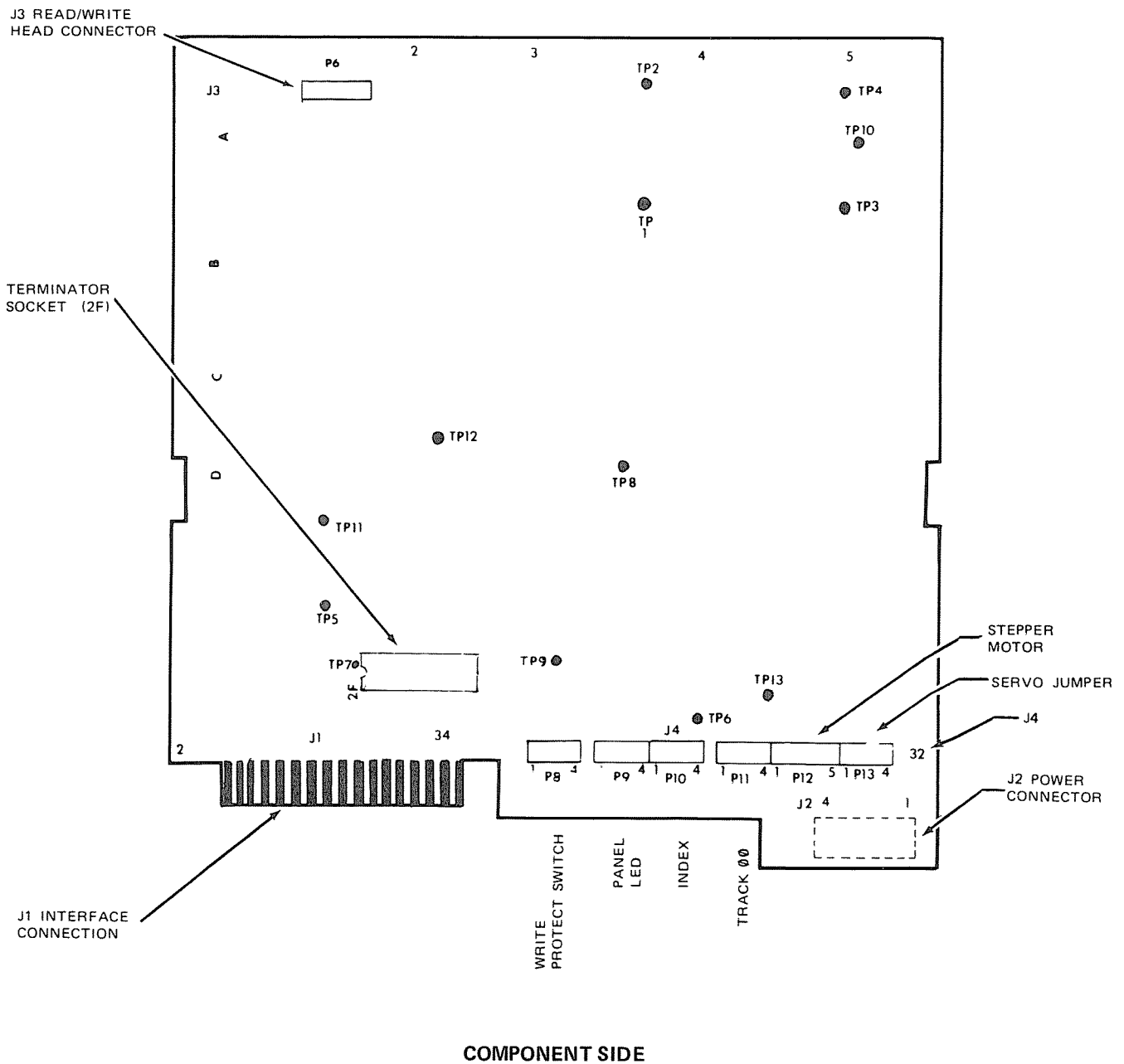
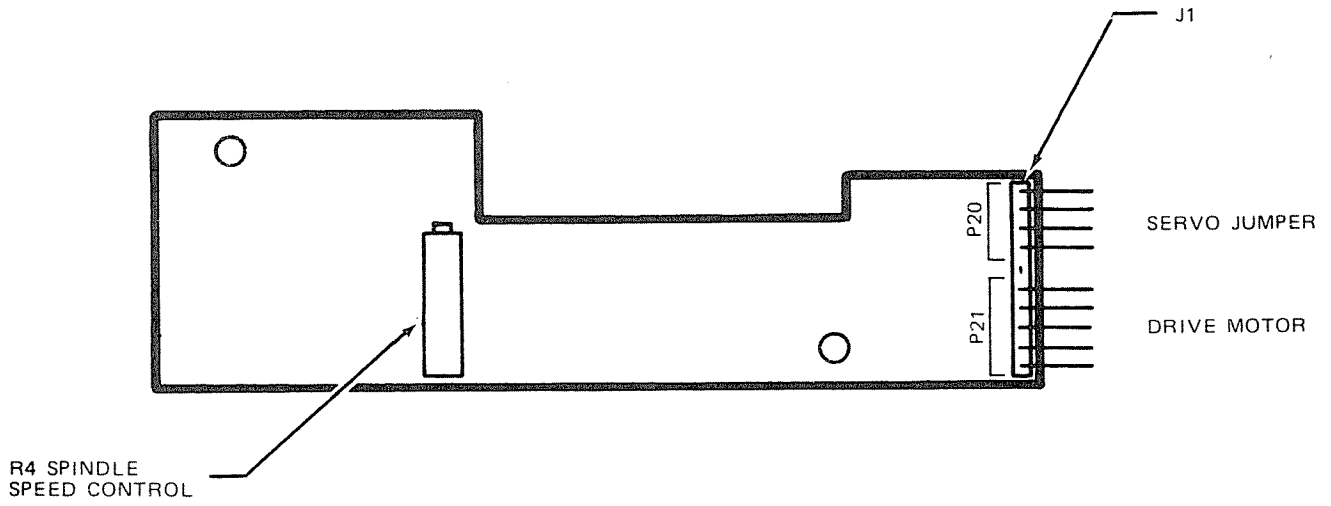
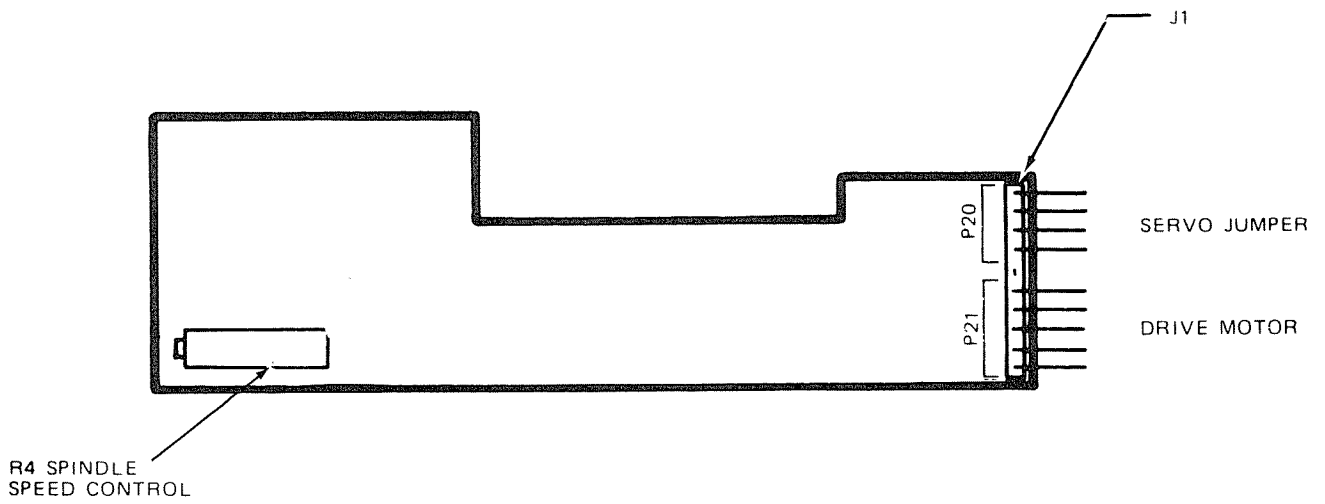


FIGURE 10. LOGIC PC BOARD TEST POINTS AND CONNECTOR LOCATIONS



NON-LINEAR SERVO BOARD (COMPONENT SIDE)



LINEAR SERVO BOARD (COMPONENT SIDE)

FIGURE 11. SERVO PC BOARD CONNECTOR LOCATIONS

D. PREVENTIVE MAINTENANCE

To ensure that the Disk Drive operates at its design potential, the only scheduled preventive maintenance required is periodic cleaning of the magnetic recording head.

Mechanical and electrical adjustment details are provided for further service as a result of disassembly or repair.

E. CLEANING THE HEAD

To clean the magnetic head, we recommend using Radio Shack's Universal Disk Drive Head Cleaning Kit, catalog number 26-407. This kit comes with complete instructions for safely cleaning the disk drive heads.

CAUTION: Rough or abrasive cloth should not be used to clean the magnetic recording head. Use of cleaning solvents other than 91% Isopropyl alcohol may damage the head.

Extreme care must be exercised to prevent the heads from being damaged (i.e., scratching, banging together, etc.).

F. ALIGNMENT AND ADJUSTMENT

To perform the alignment and adjustment procedures, you will require the following equipment:

- ★ 30 MHz Dual Trace Triggered Sweep Scope
- ★ 5 1/4" Alignment Diskette
- ★ 5 1/4" Blank "scratch" Diskette

G. DRIVE MOTOR MAINTENANCE

Long Term Motor Speed Adjustment

1. Check power to unit. (+12 VDC \pm 0.6V, and +5 VDC \pm 0.25V.)
2. Insert a blank diskette and activate the drive.
3. Under fluorescent lighting, observe the speed disk on the spindle pulley. For 60 Hz operation the outer ring on the speed disk should appear stationary. For 50 Hz operation the inner ring should appear stationary.
4. If the speed disk does not appear stationary, adjust R4, located on the Servo PCB, until the disk appears stationary.
5. If motor speed cannot be adjusted, repair Servo PCB or motor as required.

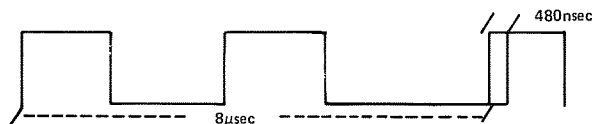
Instantaneous Speed Variation Check/RAW Data Check

1. With a blank diskette inserted, write a 2F pattern on any track.

2. Connect scope to TP 5 with:

Vert. to 2 volts/div.
Time Base to 1 μ sec/div.
Trigger internal/positive

3. Observe the waveform. Measure jitter on the leading edge of the third pulse. The leading edge of the pulse should start 8 μ sec \pm 240 nsec from the trigger pulse. The third pulse jitter should be less than 480 nsec (edge to edge).



4. If jitter is excessive, repair or replace: the drive belt, the motor; the Servo PC Board; or the spindle and bearings as necessary.

H. CARRIAGE MOVEMENT CHECK

1. Step between tracks 00 and 34/40.
2. Check carriage movement. Be certain that carriage is moving freely and not binding at any point. Repair if necessary.

I. HEAD RADIAL ALIGNMENT/CE ALIGNMENT

1. Insert a 5 1/4" alignment diskette.
2. Connect Scope:
 - Channel A to TP 1
 - Channel B to TP 2
 - Ground to TP 10
 - Ext. Sync to TP 7

Set mode to add (A + B) Invert B
 Vert. to 50 MV/div
 Trigger external - loosely.

3. Read track 16 and verify the "cat eyes" pattern as shown in Figure 12. The smaller of the two "eyes" should not be less than 75% amplitude of the other. % = (small lobe/larger lobe) x 100.

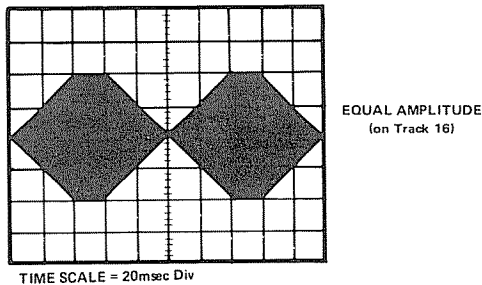


FIGURE 12. "CAT EYES" PATTERN

4. Step to track 00. Return to track 16 and re-verify the pattern.
5. Step to track 34/40 and return to track 16. Re-verify the "cat eyes" pattern.

If Radial Needs Adjustment:

- a. Loosen the two retaining screws on back of the unit and the retaining screw on the carriage assembly.
- b. Turn the Adjustment Cam until the "cat eyes" pattern is within 75%. If the pattern does not come within spec, loosen the hex head screw on the collar of the stepper motor and rotate the stepper motor shaft until the "eyes" are to the 75% level. Tighten the hex head screw and return to step a.
- c. Tighten all screws and recheck adjustment.

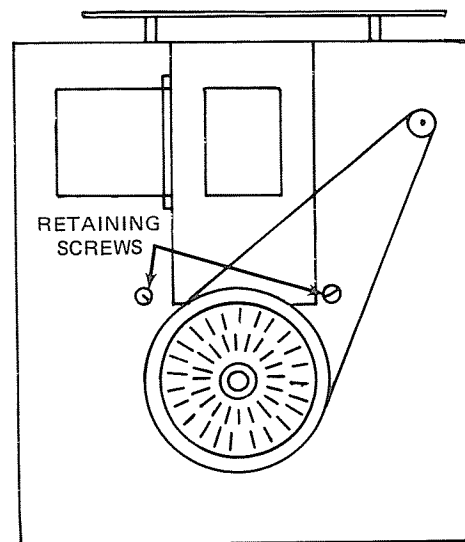
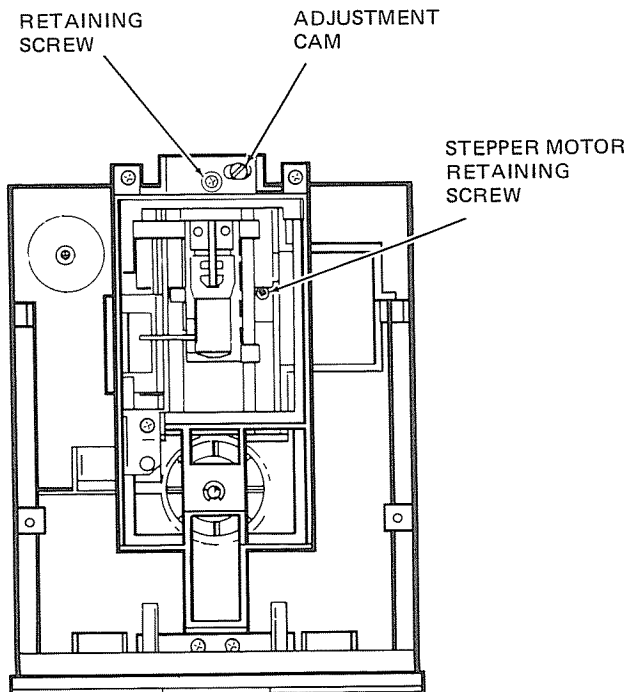


FIGURE 13. RADIAL ADJUSTMENT

J. TRACK 00 ALIGNMENT

Track 00 Switch Adjustment

1. Connect Scope:
Channel A to pin 1 of Plug 11
Vert. to 2 volts/div.
Time Base to 10 msec.
Trigger internal channel A, DC coupled
2. Step between tracks 02 and 03.
3. Loosen track 00 switch mounting screw and adjust until switch activates between tracks 02 and 03. Tighten the mounting screw.

Track 00 Stop Adjustment

1. Connect the scope as in Head Radial alignment.
2. Insert alignment diskette and read track 00.
3. Back off the track 00 stop screw two turns. Slowly turn the track 00 stop screw in until the output amplitude shown on the scope starts to decrease. Back the track 00 stop screw out until the amplitude stops increasing. Back the track 00 stop screw out one-half turn from this point.

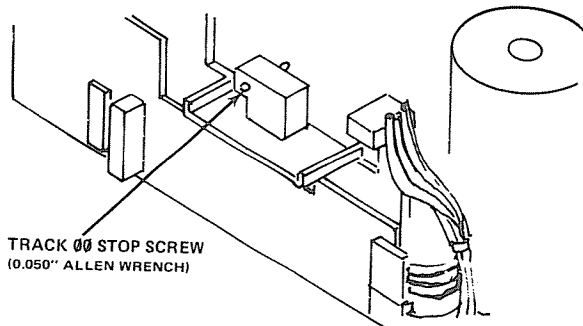


FIGURE 14. TRACK 00 STOP ADJUSTMENT

K. INDEX SECTOR ADJUSTMENT

1. Set Scope:
Vert. at 02 volts/div.
Time Base 50 μ sec/div.
2. Insert alignment diskette and read track 01. Scope display should show 0 volts AC trace for 200 μ sec \pm 50 μ sec. If the waveform is outside of spec., loosen the index sector light mounting screw and adjust to spec.
3. Open and close the Drive door and re-verify the index sector timing.

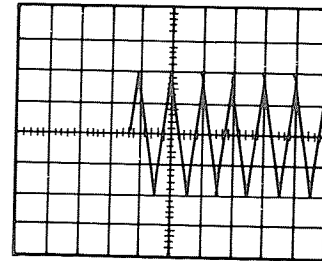


FIGURE 15. INDEX SECTOR TIMING

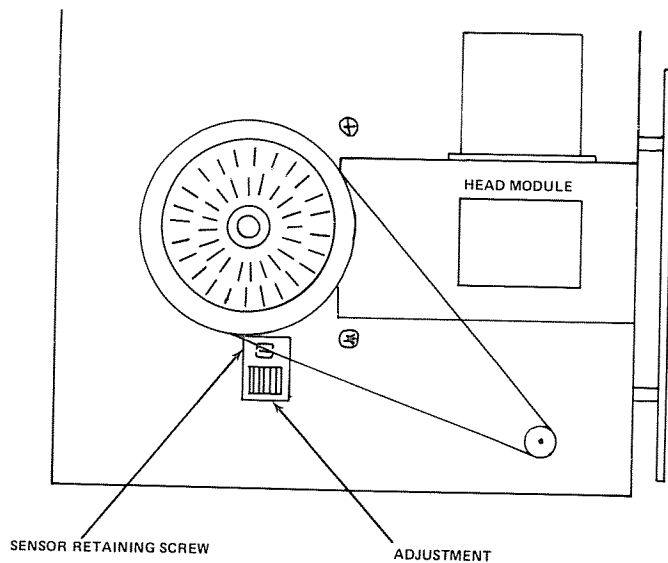


FIGURE 16. INDEX ADJUSTMENT

L. HEAD AMPLITUDE/COMPLIANCE CHECK

1. Insert a blank diskette and write a pattern to track 34.
2. Set Scope:
Time Base to $10\mu\text{sec/div}$.
Read the amplitude.
3. Apply an additional 15 grams of pressure to the head load arm. (15 grams is approximately equal to the weight of a 25 cent piece.)
4. Observe the amplitude. If it increases more than 10%, the compliance needs to be adjusted.
5. To adjust the compliance, loosen the two nuts that hold the head load arm in place. While monitoring the amplitude, move the arm until output is highest. Hold the arm in this position and tighten the nuts.
6. Re-verify compliance. If compliance cannot be adjusted properly, replace the head load arm.

M. FINAL CHECK

1. Use the drive to format and backup a blank diskette.
2. Check the diskette in a known good drive.

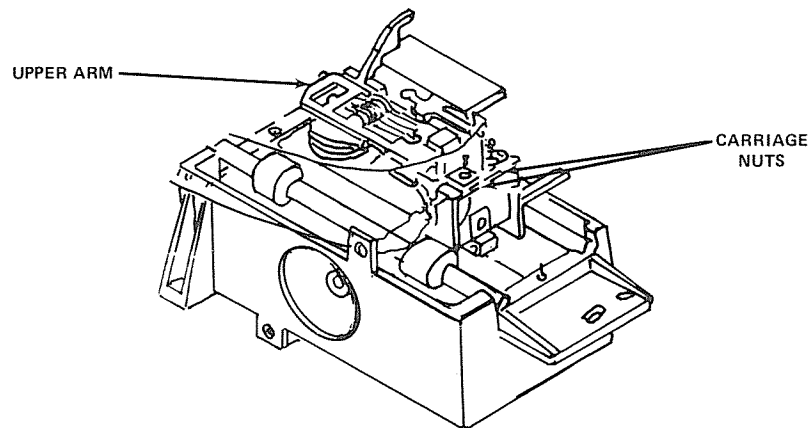


FIGURE 17. UPPER ARM AND CARRIAGE

DISK CONTROLLER BOARD PARTS LIST

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|------------|---------------------------------------|-------------------------------|----------------------------|
| CAPACITORS | | | |
| C1 | 2.2 μ F, 35V, Tantalum, Axial | 839-5223 | ACC225MGTA |
| C2 | 470pF, 50V, Monolithic | 838-1474 | ACF2124 |
| C3 | 68pF, 50V, Monolithic | 838-1684 | ACF2125 |
| C4 | 0.47 μ F, 50V, Monolithic | 838-4474 | ACF2126 |
| C5 | 0.47 μ F, 50V, Monolithic | 838-4474 | ACF2126 |
| C6 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C7 | 0.47 μ F, 50V, Monolithic | 838-4474 | ACF2126 |
| C8 | 0.47 μ F, 50V, Monolithic | 838-4474 | ACF2126 |
| C9 | 4700pF, 50V, Monolithic | 838-2474 | ACF2123 |
| C10 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C11 | 270pF, 50V, Monolithic | 838-1274 | ACF2128 |
| C12 | 470pF, 50V, Monolithic | 838-1474 | ACF2124 |
| C13 | 470pF, 50V, Monolithic | 838-1474 | ACF2124 |
| C14 | 1200pF, 50V, Monolithic | 838-2124 | ACF2127 |
| C15 | 0.1 μ F, 20V, Tantalum, Radial | 839-4102 | ACC104KETP |
| C16 | 0.1 μ F, 20V, Tantalum, Radial | 838-4102 | ACC104KETP |
| C17 | 4.7 μ F, 20V, Electrolytic, Axial | 831-5472 | ACC475MEAA |
| C18 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| ↓ | ↓ | ↓ | ↓ |
| C23 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C24 | Not Used | _____ | _____ |
| C25 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C26 | 6.8 μ F, 35V, Tantalum | 838-5683 | ACC685MGTP |
| C27 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C28 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C29 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C30 | 6.8 μ F, 35V, Tantalum | 838-5683 | ACC685MGTP |
| C31 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| ↓ | ↓ | ↓ | ↓ |
| C35 | 0.01 μ F, 50V, Monolithic | 838-3104 | ACF2130 |
| C36 | 4.7 μ F, 20V, Electrolytic, Axial | 831-5472 | ACC475MEAA |
| C37 | 4.7 μ F, 20V, Electrolytic, Axial | 831-5472 | ACC475MEAA |
| C38 | 6.8 μ F, 35V, Tantalum | 838-5683 | ACC685MGTP |
| C39 | 6.8 μ F, 35V, Tantalum | 838-5683 | ACC685MGTP |
| C40 | 330pF, 50V, Monolithic | 838-1334 | ACF2129 |
| C41 | 330pF, 50V, Monolithic | 838-1334 | ACF2129 |

DIODES

| | | | |
|------|----------|----------|---------|
| CR1 | 1N4446 | 815-0446 | ADX1364 |
| CR2 | 1N4446 | 815-0446 | ADX1364 |
| CR3 | 1N4446 | 815-0446 | ADX1364 |
| CR4 | 1N4446 | 815-0446 | ADX1364 |
| CR5 | Not Used | _____ | _____ |
| ↓ | ↓ | ↓ | ↓ |
| CR10 | Not Used | _____ | _____ |
| CR11 | 1N4446 | 815-0446 | ADX1364 |
| ↓ | ↓ | ↓ | ↓ |
| CR21 | 1N4446 | 815-0446 | ADX1364 |

**DISK CONTROLLER BOARD
PARTS LIST (Cont'd)**

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------------|---|-------------------------------|----------------------------|
| INDUCTORS | | | |
| L1 | 390 μ h | 841-9003 | ACA8058 |
| L2 | 390 μ h | 841-9003 | ACA8058 |
| L3 | 680 μ h | 841-9004 | ACA8057 |
| INTEGRATED CIRCUITS | | | |
| 3A | MC1733 | 805-0733 | AMX4326 |
| 4A | NE592A | 805-0592 | AMX3688 |
| 2B | 7406, Buffer and Interface gate | 801-0406 | AMX3675 |
| 3B | 74LS20, Positive NAND gate | 802-0020 | AMX3555 |
| 4B | 74LS20, Positive NAND gate | 802-0020 | AMX3555 |
| 5B | MSM311EL Precision Comparator | 805-3011 | AMX4327 |
| 2C | 75463, Dual Peripheral Positive OR Driver | 805-0463 | AMX4329 |
| 3C | 74123, Retriggerable Monostable Multivibrator | 800-0123 | AMX3955 |
| 4C | 74LS74, Flip-Flop | 802-0074 | AMX3558 |
| 5C | 74LS74, Flip-Flop | 802-0074 | AMX3558 |
| 3D | 74LS04, Positive NAND gate | 802-0004 | AMX3552 |
| 4D | 75462, Dual Peripheral Positive NAND Driver | 805-0462 | AMX4321 |
| 5D | 74LS86, Quadruple 2-input Exclusive OR gate | 802-0086 | AMX3701 |
| 1E | DIP Shunt, 16-pin | 848-9001 | AL0907 |
| 2E | 74LS14, Schmitt-Trigger Positive NAND gate | 802-0014 | AMX3716 |
| 3E | 7407, Buffer and Interface gate | 801-0407 | AMX3684 |
| 4E | 75462, Dual Peripheral Positive NAND Driver | 805-0462 | AMX4321 |
| 5E | 74LS221, Dual Monostable Multi- vibrator w/ Schmitt-Trigger inputs | 802-0221 | AMX3810 |
| 1F | 7438, Buffer and Interface Gate | 8000038 | AMX-3683 |
| 2F | 8-Resistor Network | 829-0007 | ARX0181 |
| 4F | 7438, Buffer and Interface Gate | 8000038 | AMX-3683 |
| RESISTORS | | | |
| R1 | 8.2K, 1/4W, 5% | 820-7282 | AN0271EEC |
| R2 | 8.2K, 1/4W, 5% | 820-7282 | AN0271EEC |
| R3 | 8.2K, 1/4W, 5% | 820-7282 | AN0271EEC |
| R4 | 27K, 1/4W, 5% | 820-7327 | AN0316EEC |
| R5 | 27K, 1/4W, 5% | 820-7327 | AN0316EEC |
| R6 | 3.6K, 1/4W, 5% | 820-7236 | AN0235BEC |
| R7 | 1K, 1/4W, 5% | 820-7210 | AN0196EEC |
| ↓ | ↓ | ↓ | ↓ |
| R12 | 1K, 1/4W, 5% | 820-7210 | AN0196EEC |
| R13 | 1.2K, 1/4W, 5% | 820-7212 | AN0199EEC |
| R14 | 150 ohms, 1/4W, 5% | 820-7115 | AN0142EEC |
| R15 | Not Used | | |
| R16 | 1K, 1/4W, 5% | 820-7210 | AN0196EEC |
| R17 | 1K, 1/4W, 5% | 820-7210 | AN0196EEC |

**DISK CONTROLLER BOARD
PARTS LIST (Cont'd)**

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|--------------------|------------------|-------------------------------|----------------------------|
| RESISTORS (cont'd) | | | |
| R18 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R19 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R20 | 750 ohms, ¼W, 5% | 820-7175 | AN0185EEC |
| R21 | 390 ohms, ¼W, 5% | 820-7139 | AN0162EEC |
| R22 | 10K, ¼W, 5% | 820-7310 | AN0281EEC |
| R23 | 390 ohms, ¼W, 5% | 820-7139 | AN0162EEC |
| R24 | 3.09K, ¼W, 5% | 820-1230 | AN0575BEC |
| R25 | 768 ohms, ¼W, 1% | 820-1176 | AN0572BEC |
| R26 | 3.9K, ¼W, 5% | 820-7239 | AN0237EEC |
| R27 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R28 | 47K, PW, 5% | 820-7347 | AN0340EEC |
| R29 | 2.2K, ¼W, 5% | 820-7222 | AN0216EEC |
| R30 | 2.2K, ¼W, 5% | 820-7222 | AN0216EEC |
| R31 | 768 ohms, ¼W, 1% | 820-1176 | AN0572BEC |
| R32 | 820 ohms, ¼W, 5% | 820-7182 | AN0187EEC |
| R33 | 390 ohms, ¼W, 5% | 820-7139 | AN0162EEC |
| R34 | 1.54K, ¼W, 1% | 820-1215 | AN0573BEC |
| R35 | 768 ohms, ¼W, 1% | 820-1176 | AN0572BEC |
| R36 | Not Used | _____ | _____ |
| ↓ | ↓ | ↓ | ↓ |
| R41 | Not Used | _____ | _____ |
| R42 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R43 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R44 | 3K, ¼W, 5% | 820-7230 | AN0226EEC |
| R45 | 10K, ¼W, 5% | 820-7310 | AN0281EEC |
| R46 | Not Used | _____ | _____ |
| R47 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R48 | 300 ohms, ¼W, 5% | 820-7130 | AN0158EEC |
| R49 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R50 | Not Used | _____ | _____ |
| R51 | Not Used | _____ | _____ |
| R52 | 150 ohms, ¼W, 5% | 820-7115 | AN0142EEC |
| R53 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R54 | 13.3K, ¼W, 1% | 820-1313 | AN0574BEC |
| R55 | 28.7K, ¼W, 1% | 820-1328 | AN0318BEC |
| R56 | Not Used | _____ | _____ |
| R57 | Not Used | _____ | _____ |
| R58 | 150 ohms, 2W, 5% | 824-7115 | AN0142EHC |
| R59 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R60 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R61 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R62 | 150 ohms, ¼W, 5% | 820-7115 | AN0142EEC |
| R63 | 10K, ¼W, 5% | 820-7310 | AN0281EEC |
| R64 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R65 | 750 ohms, ¼W, 5% | 820-7175 | AN0185EEC |
| R66 | 390 ohms, ¼W, 5% | 820-7139 | AN0162EEC |
| R67 | Not Used | _____ | _____ |
| R68 | 1K, ¼W, 5% | 820-7210 | AN0196EEC |
| R69 | 1K, ¼W, 5% | 820-7210 | AN0296EEC |

**DISK CONTROLLER BOARD
PARTS LIST (Cont'd)**

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------|--|-------------------------------|----------------------------|
| TRANSISTORS | | | |
| Q1 | 2N4124, NPN | 811-0124 | AMX4178 |
| Q2 | 2N4124, NPN | 811-0124 | AMX4178 |
| Q3 | 2N4124, NPN | 811-0124 | AMX4178 |
| Q4 | 2N4124, NPN | 811-0124 | AMX4178 |
| Q5 | 2N4125, PNP | 810-0125 | AMX4330 |
| Q6 | Not Used | _____ | _____ |
| Q7 | Not Used | _____ | _____ |
| Q8 | 2N4124, NPN | 811-0124 | AMX4178 |
| MISCELLANEOUS | | | |
| | 16-pin IC Socket (2) | 850-9003 | AJ6581 |
| | 16-pin DIP Shunt Socket | 848-9001 | AL0907 |
| | 5-pin Right Angle Header | 851-9054 | AJ6815 |
| | 14-pin Right Angle Header (2) | 851-9060 | AJ6816 |
| | Staking Pin (13) | 852-9014 | AHB9682 |
| | Resistor, \emptyset ohm vlaue – Jumper (2) | 829-0000 | AJ6814 |
| | 4-position, PC Mount Housing | 851-9056 | ART2738 |

SERVO (MOTOR CONTROL) BOARD PARTS LIST

(NON-LINEAR SERVO BOARD)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------------------|---|-------------------------------|----------------------------|
| | PRINTED CIRCUIT BOARD, SERVO (MOTOR CONTROL) | 8709096 | _____ |
| CAPACITORS | | | |
| C1 | 1.0 μ F, 35V, 20%, Tantalum | 8335103 | ACC105MGTA |
| C2 | 1.0 μ F, 35V, 20%, Tantalum | 8335103 | ACC105MGTA |
| C3 | 1.0 μ F, 35V, 20%, Tantalum | 8335103 | ACC105MGTA |
| C4 | 1.0 μ F, 35V, 20%, Tantalum | 8335103 | ACC105MGTA |
| C5 | 0.047 μ F, 80V, 10%, Tantalum | 8393474 | ACC473K KTA |
| C6 | 0.47 μ F, 35V, 20%, Tantalum | 8394473 | ACC474MGTA |
| DIODE | | | |
| CR1 | 1N4002, Rectifier, Low Power | 8150002 | ADX1148 |
| INDUCTOR | | | |
| L1 | 3.3 μ h, 10% | 8419005 | ACA8059 |
| INTEGRATED CIRCUIT | | | |
| U1 | LM2917N, Frequency to Voltage Converter | 8050917 | AMX4181 |
| RESISTORS | | | |
| R1 | 20K, 1/4 W, 5%, | 8207320 | AN0306EEC |
| R2 | 1M, 1/4 W, 5% | 8207510 | AN0445EEC |
| R3 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R4 | 1K, Trim Potentiometer | 8289210 | AP7058 |
| R5 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R6 | 43.2K, 1/4 W, 1% | 8201343 | AN0576BEC |
| R7 | 470 ohms, 1/4 W, 5% | 8207147 | AN0169EEC |
| R8 | 470 ohms, 1/4 W, 5% | 8207147 | AN0169EEC |
| R9 | 18 ohms, 1/4 W, 5% | 8207018 | AN0075EEC |
| R10 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R11 | 1 ohm, 1/2 W, 5% | 8217001 | AN0022EFC |
| R12 | 2.2K, 1/4 W, 5% | 8217222 | AN0216EEC |
| R13 | 2.2K, 1/4 W, 5% | 8217222 | AN0216EEC |
| TRANSISTORS | | | |
| Q1 | TIP110, Power | 8110110 | AMX4331 |
| Q2 | 2N4124, NPN | 8110124 | AMX4178 |
| MISCELLANEOUS | | | |
| | 10-pin, Right Angle Header | 8519057 | AJ6817 |
| | Screw, 4-40 x 1/4" (6.35 mm) | 8569032 | AHD1541 |
| | Nut, Hex, 4-40 | 8579001 | AHD7165 |

**SERVO (MOTOR CONTROL) BOARD
PARTS LIST (Cont'd)**

(LINEAR SERVO BOARD)

| SYMBOL | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|---------------------------|---|---------------------------------------|------------------------------------|
| | PRINTED CIRCUIT BOARD, SERVO (MOTOR CONTROL) | 8709169 | AXX0316 |
| CAPACITORS | | | |
| C1 | 47 μ F, 16V, Electrolytic | 8326471 | _____ |
| C2 | 47 μ F, 16V, Electrolytic | 8326471 | _____ |
| C3 | 0.1 μ F, 50V, Axial | 8374109 | _____ |
| C4 | 1.0 μ F, 35V, Tantalum | 8335103 | ACC105MGTA |
| C5 | 0.01 μ F, 80V, Axial | 8393104 | _____ |
| C6 | 0.022 μ F, 50V, Axial | 8373224 | _____ |
| INDUCTOR | | | |
| L1 | 3.3 μ h, 10% | 8419005 | ACA8059 |
| INTEGRATED CIRCUIT | | | |
| U1 | LM2917N, Frequency to Voltage Converter | 8050917 | AMX4181 |
| RESISTORS | | | |
| R1 | 20K, 1/4 W, 5% | 8207320 | AN0306EEC |
| R2 | 1M, 1/4 W, 5% | 8207510 | AN0445EEC |
| R3 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R4 | 1K, Trim Potentiometer | 8289210 | AP7058 |
| R5 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R6 | 150K, 1/4 W, 5% | 8200415 | AN0142EEC |
| R7 | 470 ohm, 1/4 W, 5% | 8207147 | AN0169EEC |
| R8 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R9 | 470 ohm, 1/4 W, 5% | 8207147 | AN0169EEC |
| R10 | 1K, 1/4 W, 5% | 8207210 | AN0196EEC |
| R11 | 1 ohm, 1/2 W, 5% | 8217001 | AN0022EFC |
| R12 | 2.2K, 1/4 W, 5% | 8217222 | AN0216EEC |
| R13 | 2.2K, 1/4 W, 5% | 8217222 | AN0216EEC |
| R14 | 1M, 1/4 W, 5% | 8207510 | AN0445EEC |
| TRANSISTORS | | | |
| Q1 | TIP110, Power | 8110110 | AMX4331 |
| Q2 | 1N4124, NPN | 8110124 | AMX4178 |
| MISCELLANEOUS | | | |
| | 10-pin, Right Angle Header | 8519057 | AJ6817 |
| | Screw, 4-40 x 1/4" (6.35 mm) | 8569032 | AHD1541 |
| | Nut, Hex, 4-40 | 8579001 | AHD7165 |

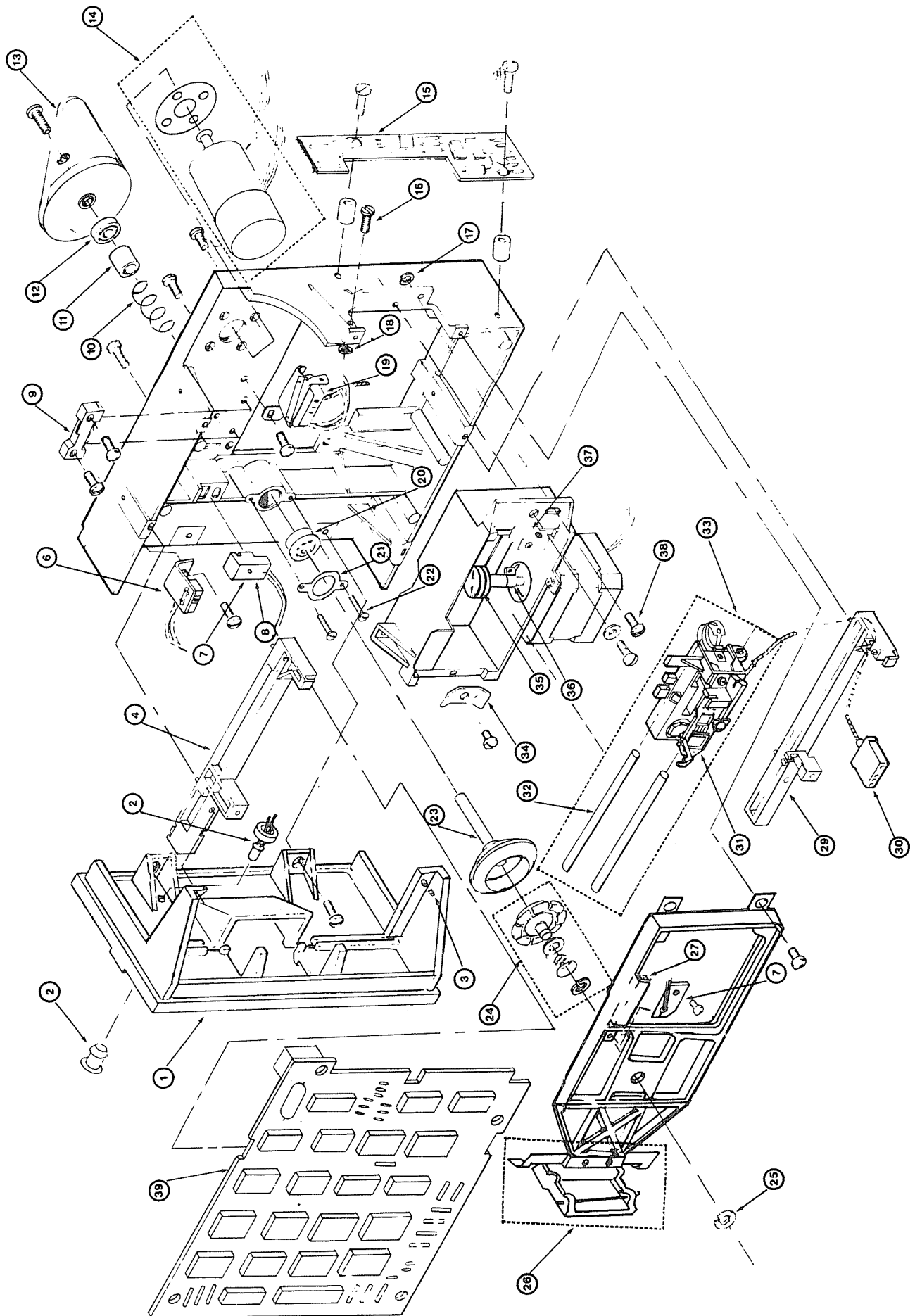
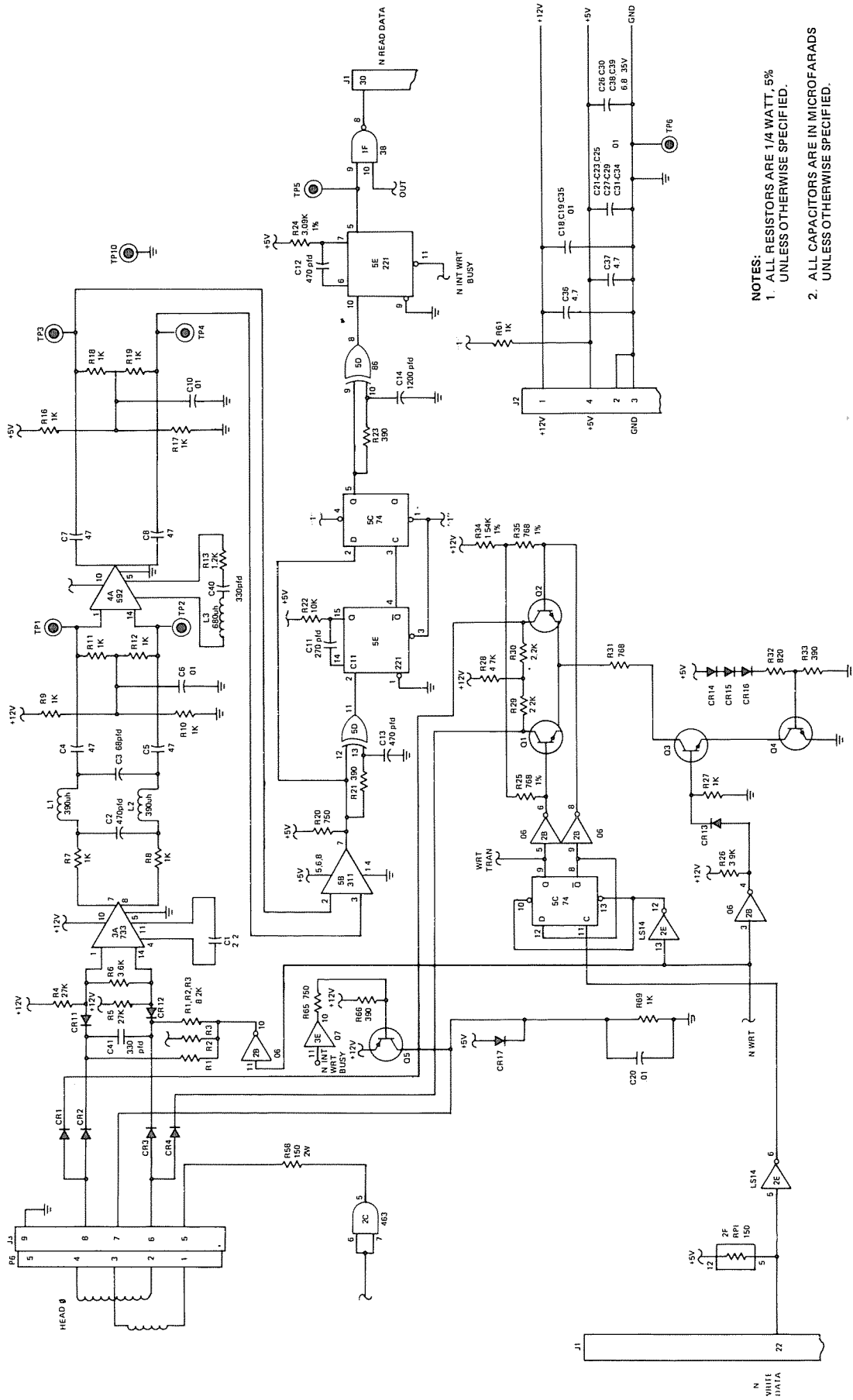


FIGURE 18. ILLUSTRATED PARTS – EXPLODED VIEW

**PARTS LIST
ILLUSTRATED PARTS CATALOG**

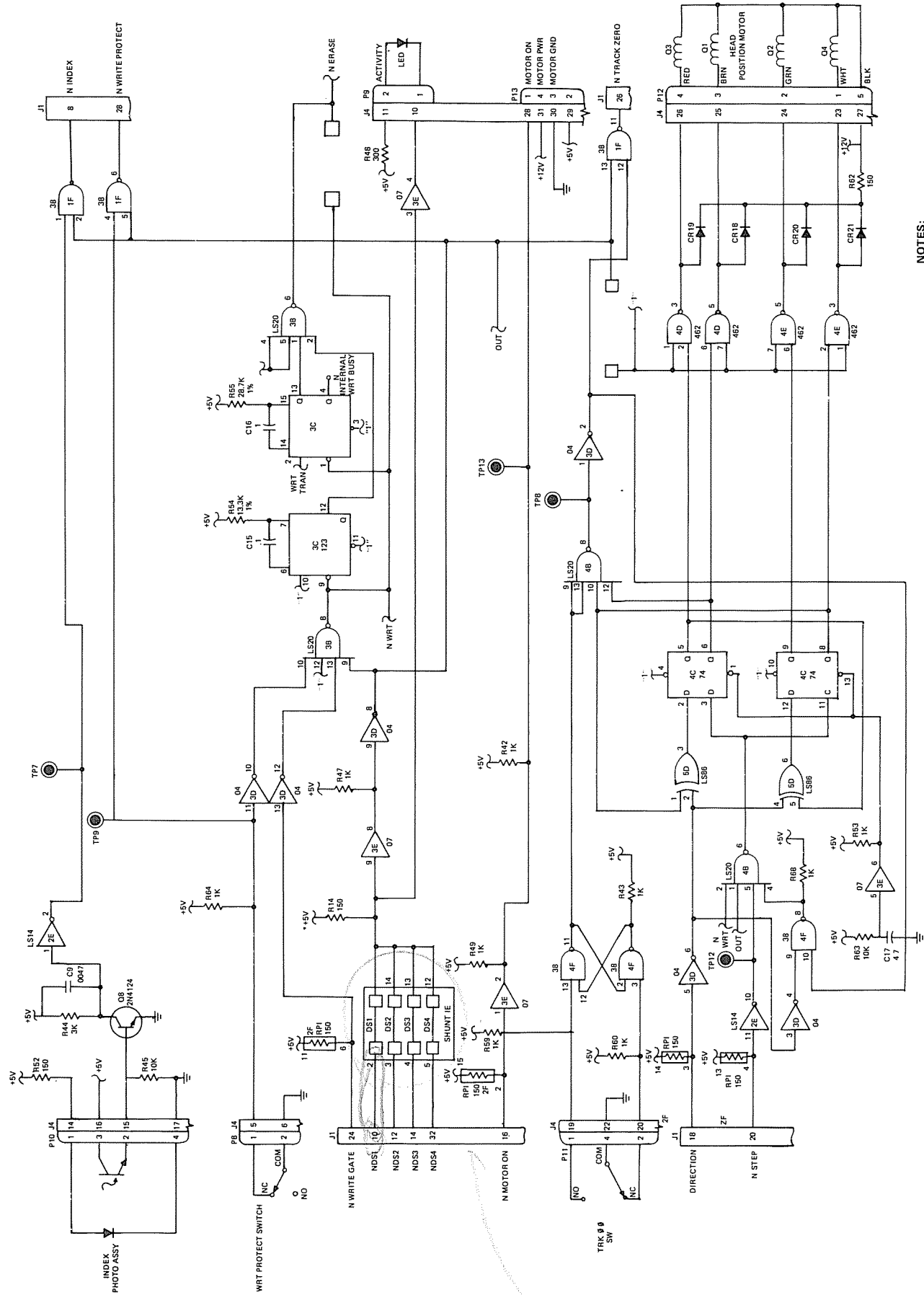
| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|--|-------------------------------|----------------------------|
| 1 | Front Panel | 8852025 | AZ5380 |
| 2 | LED Assembly (Panel) | 8852020 | AL1127 |
| 3 | Front Panel Bushing | 8852026 | AHB9684 |
| 4 | Left Hand Guide | 8852024 | ART2743 |
| 6 | Write Protect Switch Assembly | 8852017 | AS2587 |
| 7 | Index Assembly, Type I | 8852019 | ART2739 |
| | Type II* | 8852043 | ART2895 |
| 8 | Detector Holder | 8852048 | ART3003 |
| 9 | Module Bias Spring Assembly | _____ | _____ |
| 10 | SSR Spring | 8852060 | ARB6845 |
| 11 | SSR Spring Housing | 8852059 | ART3006 |
| 12 | Lower Bearing | 8852028 | ART2745 |
| 13 | Drive Belt | 8852018 | AB6443 |
| 14 | Drive Motor Assembly | 8852015 | AM4545 |
| 15 | Servo Board, non-linear | 7000008 | AXX0316 |
| | linear | 7000006 | _____ |
| 16 | Track $\emptyset\emptyset$ Screw | 8852057 | AHD1601 |
| 17 | E-ring, large (cam) | 8852049 | AHE0029 |
| 18 | E-ring, small (Track $\emptyset\emptyset$) | 8852051 | AHE0031 |
| 19 | Track $\emptyset\emptyset$ Switch Assembly | 8852016 | AS2586 |
| 20 | Upper Bearing | 8852027 | ART2744 |
| 21 | Hub Retainer | 8852055 | AHB9985 |
| 22 | Hub Retainer Screw | 8852056 | AHD1600 |
| 23 | Machined Hub Assembly | _____ | ART2740 |
| 24 | Cone Assembly (2 pcs.) | 8852021 | ART3511 |
| 25 | E-ring, medium (cone) | 8852050 | AHE0030 |
| 26 | Latch Assembly | 8852022 | ADA0303 |
| 27 | Foam Cone Lever Pad | 8852063 | AHB9986 |
| 29 | Right Hand Guide | 8852023 | ART2742 |
| 30 | Crimp Pin (tin) | 8852045 | AHB9982 |
| | (gold) | 8852046 | AHB9983 |
| | (inside Head Plug) | | |
| 31 | Upper Arm Assembly | 8852044 | ART3002 |
| 32 | Carriage Shaft | 8852065 | ART3050 |
| 33 | Head Carriage Assembly | 8852031 | AH4403 |
| 34 | Shaft Mounting Clamp | 8852064 | AHC0048 |
| 35 | Drive Band, (Stepper) | 8852032 | ART2746 |
| 36 | Collar, (Stepper) | 8852047 | AHB9984 |
| 37 | Track $\emptyset\emptyset$ Stop Kit | 8852052 | ART3004 |
| 38 | Module Cam Screw | 8852058 | AHD1602 |
| 39 | Logic PC Board | 7000007 | AXX0317 |
| not shown | Module Cover, clear plastic | 8852062 | ART3007 |
| | Cone Lever Assembly | 8852053 | ART3005 |
| | includes: cone assembly, E-ring, med., latch assembly, and foam cone lever pad | | |
| | Module Assembly SSR | 8852029 | AXX0318 |
| | includes: upper arm assembly, carriage shaft, head carriage assembly, shaft mounting clamp, drive band, collar, track $\emptyset\emptyset$ stop kit, and module cam screw | | |

*Type II Assemblys have a gold band around the photo transistor.



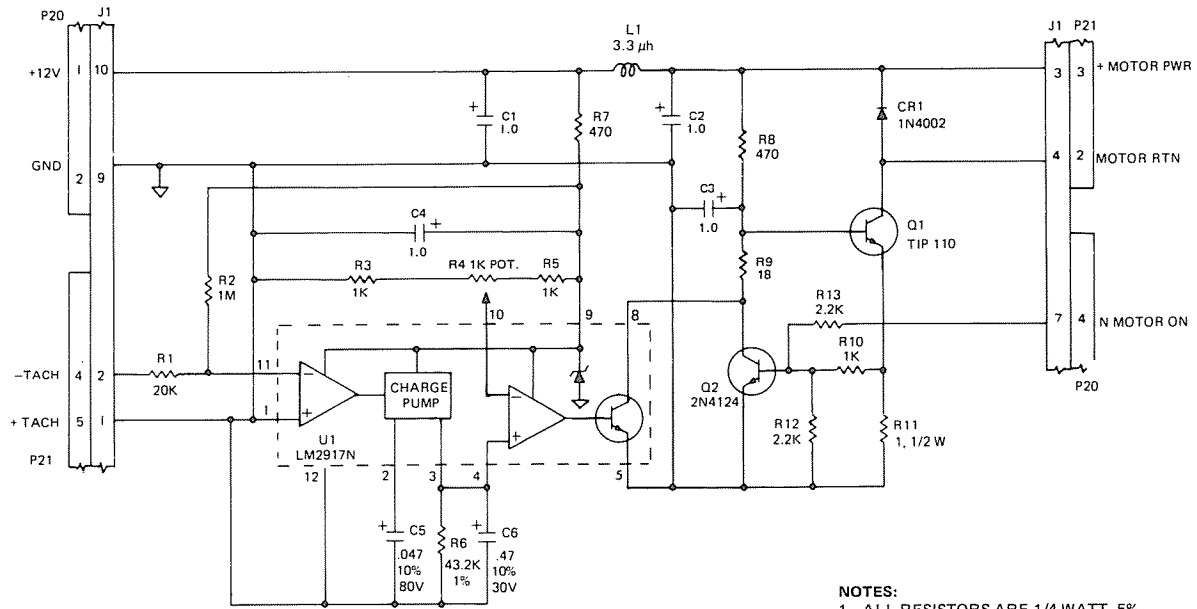
NOTES:
 1. ALL RESISTORS ARE 1/4 WATT, 5% UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

FIGURE 19. MINI-DISK DRIVE SCHEMATIC DIAGRAM (Sheet 1)



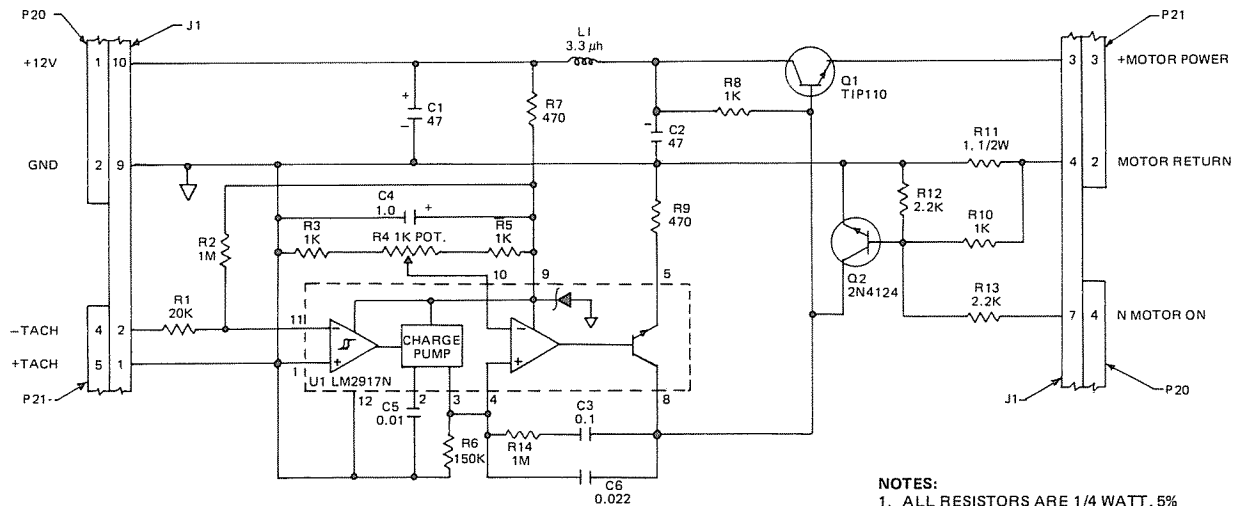
- NOTES:
1. ALL RESISTORS ARE 1/4 WATT, 5% UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

FIGURE 19. MINI-DISK DRIVE SCHEMATIC DIAGRAM (Sheet 2)



- NOTES:**
1. ALL RESISTORS ARE 1/4 WATT, 5% UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

NON-LINEAR SERVO BOARD



- NOTES:**
1. ALL RESISTORS ARE 1/4 WATT, 5% UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED.

LINEAR SERVO BOARD

FIGURE 20. SERVO PC BOARD SCHEMATIC DIAGRAM

SUPPLEMENT TO SECTION IX

THIS SUPPLEMENT APPLIES TO ALL DISK DRIVES (26-1160 TO 26-1164) THAT USE THE NEW SINGLE (LOGIC/SERVO) BOARD DRIVE CIRCUITRY. THE CIRCUITRY HAS BEEN UPDATED AND NEW TEST POINTS ARE USED, ALTHOUGH ALL MECHANICAL ADJUSTMENTS WILL REMAIN THE SAME AS THE PREVIOUS TWO BOARD SYSTEMS.

SECTION I

GENERAL DESCRIPTION

A. INTRODUCTION

The main difference is in the PC Board (there is only one board, the Servo Motor circuitry has been incorporated onto the Logic Board and the DIP Resistor Termination and IC Socket have been replaced by a SIP Resistor Termination package and Socket). A changed paragraph is indicated by a vertical line in the margin adjacent to that paragraph. The Figure numbers in this section correspond to the Figures in the Manual.

B. PHYSICAL DESCRIPTION

The electronic components are mounted on the Logic/Servo Board. The Logic/Servo Board is located above the chassis, and the Power and interface signals are connected directly to that Board.

The spindle is belt driven by a DC motor with an integral tachometer. The servo control circuit, pulleys and the tachometer control the speed of the spindle. The read/write/erase head assembly is positioned by means of a stepper motor, split band and a pulley.

C. FUNCTIONAL DESCRIPTION

The Disk Drive is fully self-contained. It consists of a spindle drive system, a head positioning system, and read/write/erase system.

When the front latch is opened, access is provided for the insertion of a 5.25 inch (133.4 mm) standard diskette. The diskette is positioned in place by plastic guides, the front latch and a back stop.

Closing the front latch activates the cone/clamp system which centers and clamps the diskette to the drive hub. The drive hub is driven at a constant speed of 300 rpm by a servo controlled DC motor. In operation, the magnetic head is loaded into contact with the recording medium whenever the front latch is closed.

A 4-phase stepper motor/band assembly and its associated electronics position the magnetic head over the desired track. This positioner employs a one-step rotation to cause a 1-track linear movement. When a write-protected diskette is inserted into the Drive, the write-protect sensor disables the write electronics of the Drive and an appropriate signal is applied to the interface. (When performing a write operation, a 0.013-inch (0.33 mm) [nominal] data track is recorded.)

Data recovery electronics include a low-level read amplifier, differentiator, zero-crossing detector and digitizing circuits. No data decoding facilities are provided in the basic Drive.

The Drive is also supplied with the following sensor systems:

1. A track $\emptyset\emptyset$ switch senses when the Head/Carriage assembly is positioned at Track $\emptyset\emptyset$.
2. The index sensor (an LED light source and a photo-transistor) is positioned so that when an index hole is detected, a digital signal is generated. The index sensor used is a high resolution device which can distinguish holes placed close together, i.e., index-sector holes in a hard sectored diskette.
3. The write-protect sensor disables the Disk Drive electronics whenever a write-protect tab is applied to the diskette.

D. INTERFACE CONNECTIONS

Signal connections for the external Disk Drive are made via a user-supplied 34-pin flat ribbon connector. The internal Drive uses a Radio Shack connector, Part Number AW2535. Both of these connectors mate directly with the PC Board connector (J2) at the rear of the Drive. The DC power connector is a four-pin connector (J4) on the PC Board at the top rear of the Drive.

The signal connector harness should be of the flat ribbon or twisted pair type with the following characteristics:

1. Maximum length of 10 feet (3 M).
2. 22 - 24 gauge conductor compatible with the connector to be used.

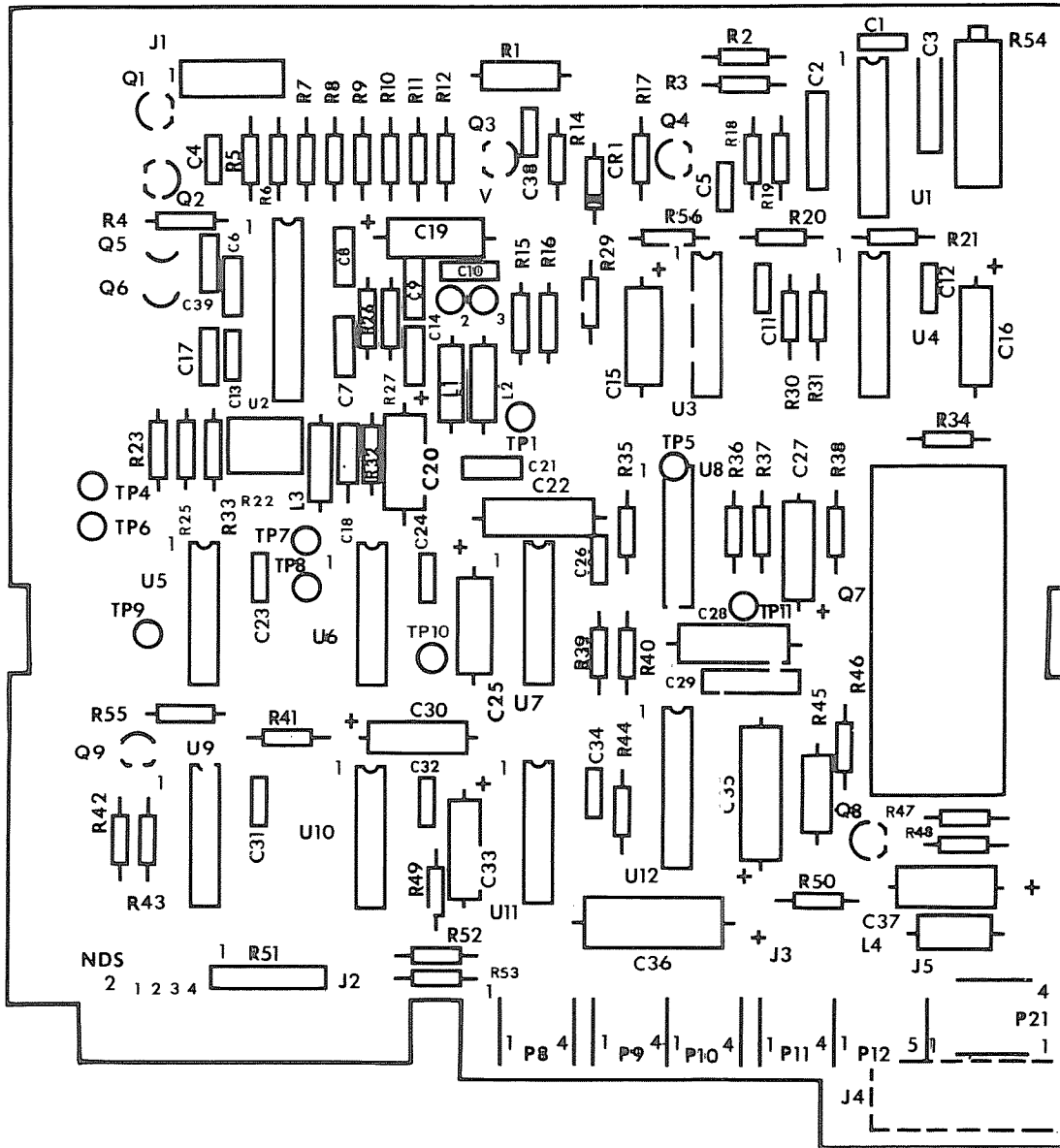
Power connections for external Drives should be made with 18 AWG cable. Internal Drives use the Disk DC Power Harness, Radio Shack Part Number AW2532.

E. PHYSICAL CHECKOUT

Before applying power to the unit, the following inspection should be performed:

1. Front latch. Check that the front latch opens and closes. Note that when the door is opened, the head arm is raised.
2. Ensure that the front panel is secure.
3. Manually rotate the drive hub. The hub should rotate freely.
4. Check that the PC Board is secure. Check that the connectors are firmly seated.
5. Check for debris or foreign material between the heads and remove same.
6. Check plastics for broken or cracked pieces, e.g., write-protect lever, guide rails, etc.

NOTE: To ensure proper operation of the Drive, the chassis should be connected to earth ground. The 3/16-inch (4.76 mm) male QC lug, located at the rear of the chassis, is provided for this connection.



LOGIC BOARD (COMPONENT SIDE)

FIGURE 2. LOGIC/SERVO PC BOARD COMPONENT LOCATIONS

F. MOUNTING THE DISK DRIVE

The Drive can be mounted in any plane, i.e. upright, horizontal or vertical. However, when it is mounted horizontally, the Logic PC board side of the chassis must be the uppermost side. Tapped holes are provided in various locations for the attachment of user-supplied hardware.

G. FLAT RIBBON CABLE ASSEMBLY

The Flat Ribbon Cable Assembly that is used with the redesigned P.C. Board can be used with either the Model I or Model III Computers. Refer to Section I, General Description FLAT RIBBON CABLE ASSEMBLY for Connector pin configuration.

H. RESISTOR TERMINATION

(See Figure 3)

The Resistor Termination in the SIP socket (R51) is used only in the last drive in the system. Remove all other Resistor Terminations.

NOTE: The internal drives in the Model III Computer are not terminated.

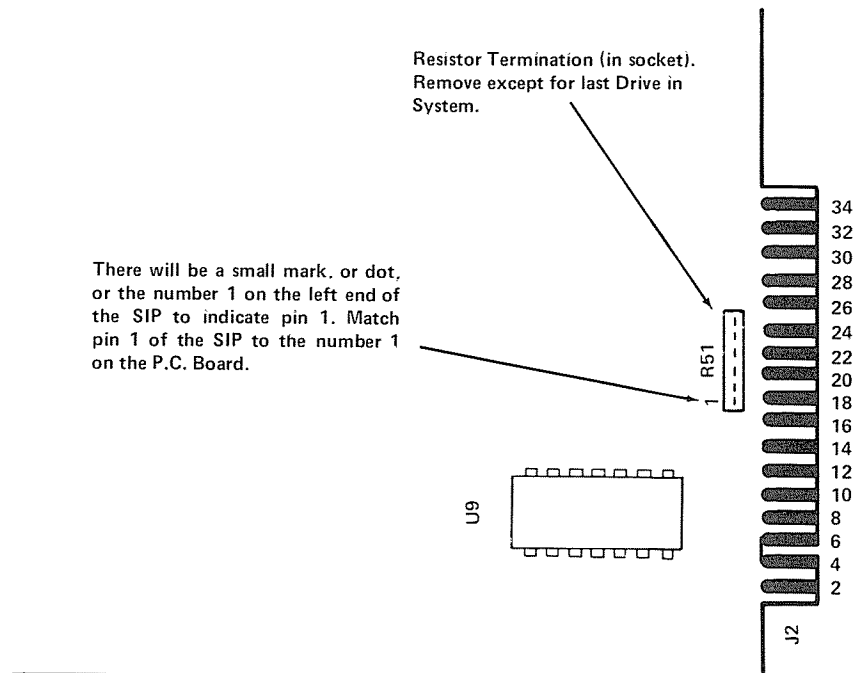


FIGURE 3. RESISTOR TERMINATION

J. DATA RECORDING

Referring to Figure 5 it can be seen that the Write Electronics consists of a Write/Erase Current Source and Write Waveform Generator, Erase Current Source, and Trim Erase Control Logic.

The read/write winding on the magnetic head is center-tapped. During a write operation, current from the Write Current Source flows in alternate halves of the winding under control of the Write Waveform Generator.

Before recording can begin, certain conditions must be satisfied. The conditions required for recording (i.e., unit ready) must be established by the user system as follows:

- (1) Drive speed stabilization. This condition will exist 250 mSec after starting the drive motor.
- (2) Subsequent to any step operation, the positioner must be allowed to settle. This requires 20 mSec total after the last step pulse is initiated, i.e., 5 mSec for the step motion and 15 mSec for settling.

NOTE: All of the foregoing operations can be overlapped, if required.

Figure 7 shows the relevant timing diagram for a write operation. When $t=0$, the unit is ready and the WRITE ENABLE interface line goes true thus enabling the Write Current Source.

Since the trim erase gaps are behind the read/write gap, TRIM ERASE control goes true 390 μ Sec after the WRITE ENABLE interface line. It should be noted that this value is optimized between the requirements at Track 00 and Track 40 so that the effect of the trim erase gaps on previous information is minimized.

Figure 7 also shows the information on the WRITE DATA interface line and the output of the Write Waveform Generator which toggles on the leading edge of every WRITE DATA pulse.

Note that a minimum of 4 μ Sec and a maximum of 8 μ Sec between WRITE ENABLE going true and the first WRITE DATA pulse is only required if faithful reproduction of the first WRITE DATA transition is significant.

At the end of recording, at least one additional pulse on the WRITE DATA line must be inserted after the last significant WRITE DATA pulse to avoid excessive peak shift effects.

The TRIM ERASE signal must remain true for 800 μ Sec after the termination of WRITE ENABLE to ensure that all recorded data are trim erased. This value is again optimized between the requirements at Tracks 00 and 40.

The duration of a write operation is from the true-going edge of WRITE ENABLE to the false-going edge of TRIM ERASE. This is indicated by the internal WRITE BUSY waveform shown.

K. DATA REPRODUCTION

The Read electronics consists of the following:

- ★ Read Switch
- ★ Read Amplifier
- ★ Filter
- ★ Differentiator
- ★ Comparator and Digitizer

The Read Switch consists of two FETs that are used to isolate the Read Amplifier from electrical signals across the magnetic head during a Write operation.

The remaining functions of the Read circuitry are contained in the MC 3470 IC.

Before reading can begin, the Drive must be in a ready condition. As with the data recording operation, this ready condition must be established by the user system. In addition to the requirements established in the paragraph, DATA RECORDING, a 100 μ Sec delay must exist from the trailing edge of the TRIM ERASE signal to allow the Read Amplifier to settle after the transient caused by the Read Switch returning to the Read mode.

Referring to Figure 8 the output signal from the read/write head is amplified by a read amplifier and filtered to remove noise by a linear phase Filter. The linear output from the Filter is passed to the Differentiator which generates a waveform whose zero crossovers correspond to the peaks of the read signal. This signal is then fed to the Comparator and Digitizer circuit. Variable Resistor R22 is used to balance the Comparator and Differentiator by adjusting out any circuit imbalances and reducing peak shift.

The Comparator and Digitizer circuitry generates a 1 μ Sec READ DATA pulse corresponding to each peak of the read signal. This Composite Read Data signal is then sent to the user system via the READ DATA interface line.

SECTION III

OPERATION

A. INTRODUCTION

This section contains the interface description and the electrical adjustments necessary for the Disk Drive.

B. INTERFACE ELECTRONICS SPECIFICATIONS

All interface signals are TTL compatible. Logic true (low) is +0.4 V (maximum). Logic false (high) is +2.4 V (minimum). Figure 9 illustrates the interface configuration.

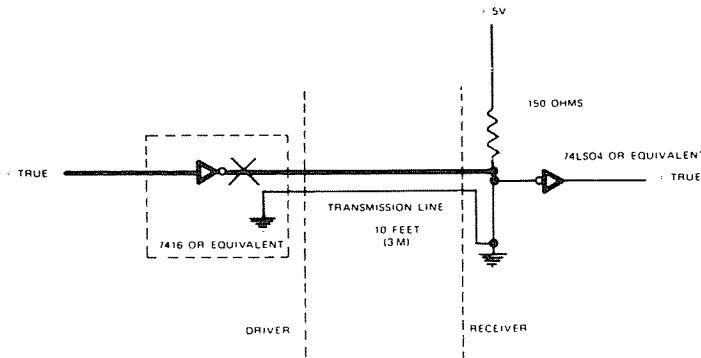


FIGURE 9. INTERFACE CONFIGURATION

It is recommended that the interface cable be a flat ribbon cable, with a characteristic impedance of 100 ohms. (or equivalent twisted pairs). Maximum interface cable length is 10 feet (3 M).

C. INPUT CONTROL LINES

Interface connector pin assignments and power connector pin assignments are given in Table 2 and Table 3 in Section III of the Manual.

D. SELECT LINES (DS1* - DS4*)

The SELECT lines provide a means of selecting and deselecting a Disk Drive. These four lines (DS1* - DS4*) select one of the four Disk Drives attached to the controller. When the signal logic level is true (low), the Disk Drive electronics are activated and the Drive is conditioned to respond to step or read/write commands. When the logic level is false (high) the input control lines and output status lines are disabled.

A SELECT line must remain stable in the true (low) state until the execution of a step or read/write command is completed.

The Disk Drive address is determined by SELECT lines 1 through 4 on the PC Board. These lines provide a means of daisy-chaining a maximum of four Disk Drives to a controller. Only one line can be true (low) at a time. An undefined operation might result if two or more units are assigned the same address or if two or more SELECT lines are in the true (low) state simultaneously.

E. DRIVE MOTOR ENABLE (MOTORON)

When this signal line logic level goes true (low), the drive motor accelerates to its nominal speed of 300 rpm and stabilizes in less than 250 mSec. When the logic level goes false (high), the Disk Drive decelerates to a stop.

F. DIRECTION AND STEP (DIR*) (STEP*)

When the Disk Drive is selected, a true (low) pulse with a time duration greater than 200 nSec on the STEP line initiates the access motion. The direction of motion is determined by the logic state of the DIRECTION line when a STEP pulse is issued. The motion is towards the center of the disk if the DIRECTION line is in the true (low) state when a STEP pulse is issued. The direction of motion is away from the center of the disk if the DIRECTION line is in the false (high) state when a STEP pulse is issued. To ensure proper positioning, the DIRECTION line should be stable 0.1 μ Sec (minimum) before the trailing edge of the corresponding STEP pulse and remain stable until 0.1 μ Sec after the trailing edge of the STEP pulse. The access motion is initiated on the trailing edge of the STEP pulse.

G. COMPENSATED WRITE DATA (CWD)

When the Disk Drive is selected, this interface line provides the bit-serial WRITE DATA pulses that control the switching of the write current in the head. The write electronics must be conditioned for writing by the WRITE ENABLE line (refer to the WRITE ENABLE paragraph below).

For each high-to-low transition on the WRITE DATA line, a flux change is produced at the head write gap. This causes a flux change to be stored on the disk.

When the double-frequency type encoding technique is used (in which data and clock form the combined Write Data signal), it is recommended that; when writing all zeroes, the repetition rate of the high-to-low transitions be equal to the nominal data rate, $\pm 0.1\%$. The repetition rate of the high-to-low transitions, when writing all ones, should be equal to twice the nominal data rate, $\pm 0.1\%$.

H. WRITE GATE (WG*)

When this signal is true (low), the write electronics are prepared for writing data (read electronics disabled). This signal turns on write current in the read/write head. Data is written under control of the WRITE DATA input line. It is generally recommended that changes of state on the WRITE ENABLE line occur before the first WRITE DATA pulse. However, the separation between the leading edge of WRITE ENABLE and the first significant WRITE DATA pulse should not be less than 4 μ Sec and not greater than 8 μ Sec. The same restrictions exist for the relationship between the least significant WRITE DATA pulse and the

SECTION IV MAINTENANCE

A. PHYSICAL DESCRIPTION OF THE PC BOARD

The Logic/Servo board is approximately 6 inches (152 mm) long by 5.5 inches (139 mm) wide. Figure 10 illustrates the placement of test points and connectors.

INSTALLATION

To replace the Logic P.C. Board and the Servo P.C. Board with the newer Logic/Servo P.C. Board, the following steps should be taken:

1. Discard the jumper cable that goes from P13 on the Logic P.C. Board to P20 on the Servo P.C. Board.
2. Disconnect all cables that connect the two Boards.
3. Remove both the Logic and the Servo P.C. Boards and the Servo P.C. Board mounting hardware.
4. Connect all cables except the Drive Motor Cable that was connected to P21 on the Servo P.C. Board.
5. Connect the Drive Motor Cable to P13 on the Logic/Servo P.C. Board.
6. Go through the maintenance checks again. Pay particular attention to Part H., DRIVE MOTOR MAINTENANCE and Part N., PEAK SHIFT COMPENSATION ADJUSTMENT.

B. CIRCUIT BOARD TEST POINTS

The following test point description assumes that the Logic/Servo P.C. Board is installed in the Drive and that the Drive is in an operational mode with a diskette installed:

Analog Ground (TP1)

The analog ground reference point is provided for measuring read/write waveforms.

Amplified Read Signal (TP2, TP3)

These test points are provided to observe the differential output of the first stage of read signal amplification.

Logic Ground (TP4)

Digital Logic ground is referenced at TP4.

Track 00 (TP5)

This signal is low (true) when the carriage is positioned at track 00 and the step motor phase is correct.

Step Pulse (TP6)

When stepping in or out, the signal is a high-going pulse for each step of the carriage.

Read Data One Shot (TP7)

The output of the one shot used in the read section is nominally 1.0 μ sec for each flux transition detected.

Write Protect Switch (TP8)

When a write protected diskette is installed in the Drive, the signal is low (true).

Index Pulse (TP9)

With a standard soft sectored diskette installed, the signal is a high going-pulse, nominally 4.0 msec in duration every 200 msec.

Motor On (TP11)

This signal is low (true) for the Motor On condition.

C. OPTION SELECT

Input Line Terminations

The Disk Drive has been provided with the capability of terminating the input lines listed below:

- ★ Motor On
- ★ Direction Select
- ★ Step
- ★ Write Data
- ★ Write Gate

These lines are terminated through a 150 ohm resistor pack that is installed in a SIP socket (R51), located adjacent to J2.

In a multiple drive system, only the last drive on the interface is to be terminated. All other drives on the interface must have the resistor pack removed. Catalog Numbers 26-1160 and 26-1164 are shipped with the termination resistor installed. Catalog Numbers 26-1161/1162/1163 are shipped without a resistor pack.

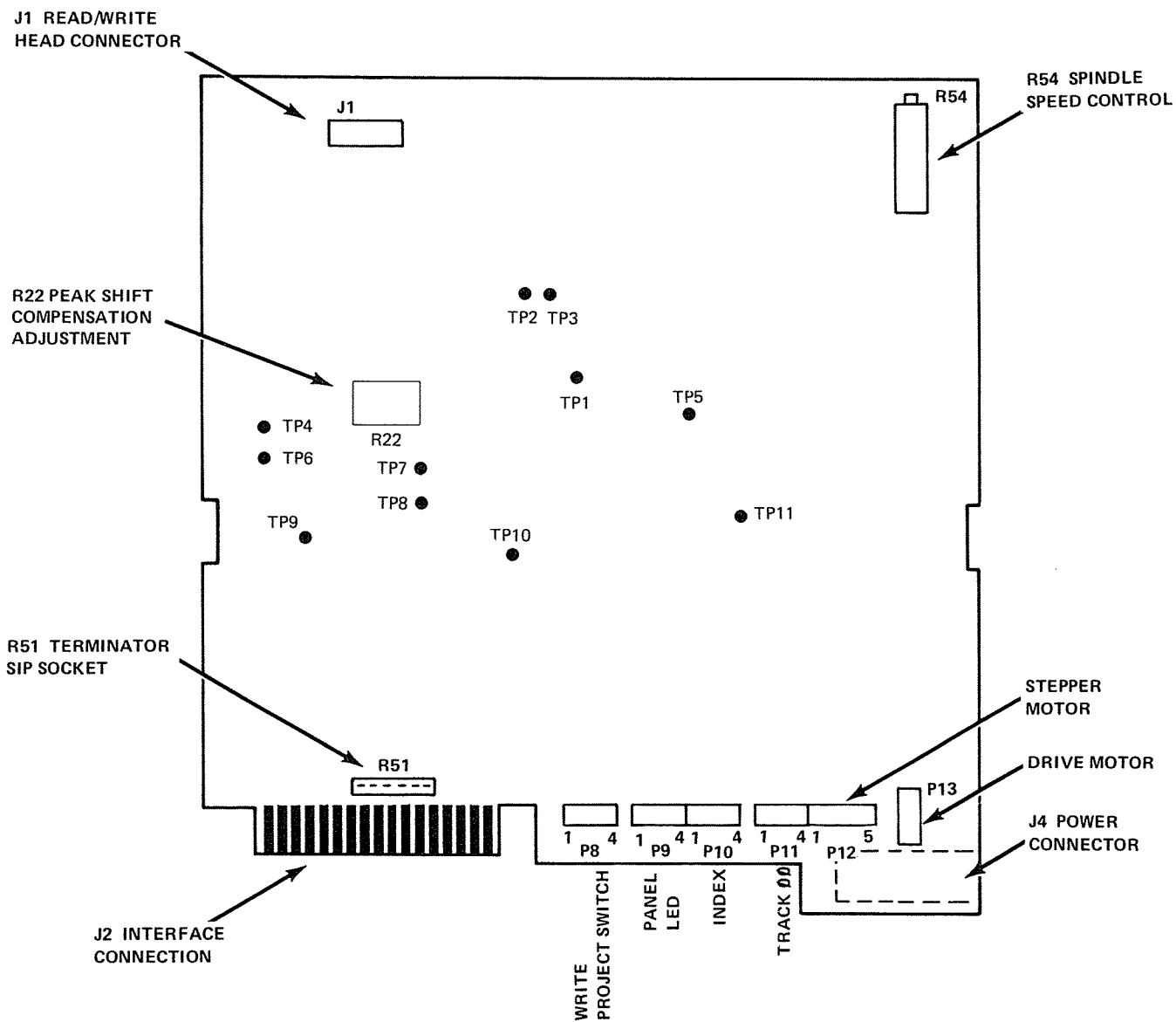


FIGURE 10. LOGIC/SERVO PC BOARD TEST POINTS AND CONNECTOR LOCATIONS

D. PREVENTIVE MAINTENANCE

To ensure that the Disk Drive operates at its design potential, the only scheduled preventive maintenance required is periodic cleaning of the magnetic recording head.

Mechanical and electrical adjustment details are provided for further service as a result of disassembly or repair.

E. CLEANING THE HEAD

To clean the magnetic head, we recommend using Radio Shack's Universal Disk Drive Head Cleaning Kit, catalog number 26-407. This kit comes with complete instructions for safely cleaning the disk drive heads.

CAUTION: Rough or abrasive cloth should not be used to clean the magnetic recording head. Use of cleaning solvents other than 91% Isopropyl alcohol may damage the head.

Extreme care must be exercised to prevent the heads from being damaged (i.e., scratching, banging together, etc.).

F. ALIGNMENT AND ADJUSTMENT

To perform the alignment and adjustment procedures, you will require the following equipment:

- ★ 30 MHz Dual Trace Triggered Sweep Scope
- ★ 5 1/4" Alignment Diskette
- ★ 5 1/4" Blank "scratch" Diskette

G. DRIVE MOTOR MAINTENANCE

Long Term Motor Speed Adjustment

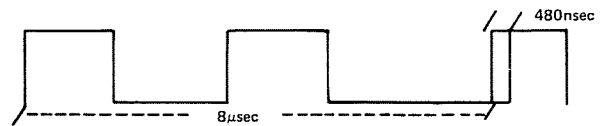
1. Check power to the unit. (+12 VDC ± 0.6 V, and +5 VDC ± 0.25 V.)
2. Insert a blank diskette and activate the drive.
3. Under fluorescent lighting, observe the speed disk on the spindle pulley. For 60 Hz operation, the outer ring on the speed disk should appear to be stationary. For 50 Hz operation, the inner ring should appear stationary.
4. If the speed disk does not seem to be motionless, adjust R54 (located in the upper right corner of the PC Board) for the desired effect.
5. If motor speed cannot be adjusted, repair the PC Board or the motor as required.

Instantaneous Speed Variation Check/RAW Data Check

1. With a blank diskette inserted, write a 2F pattern on any track.
2. Connect the 'scope to TP7 with:

Vert. to 2 volts/div.
Time Base to 1 μ sec/div.
Trigger internal/positive

3. Observe the waveform. Measure jitter on the leading edge of the third pulse. The leading edge of the pulse should start 8 μ sec ± 240 nsec from the trigger pulse. The third pulse jitter should be less than 480 nsec (edge to edge).



4. If jitter is excessive, repair or replace the drive belt, motor, PCB, or spindle as necessary.

H. CARRIAGE MOVEMENT CHECK

1. Step between tracks 00 and 34/40.
2. Check carriage movement. Be certain that carriage is moving freely and not binding at any point. Repair if necessary.

I. HEAD RADIAL ALIGNMENT/CE ALIGNMENT

1. Insert a 5 1/4" alignment diskette.
2. Connect Scope:
 - Channel A to TP2
 - Channel B to TP3
 - Ground to TP1
 - Ext. Sync. to TP9

Set mode to add (A + B) Invert B
 Vert. to 20 mV/Div
 Trigger external - loosely.

3. Read track 16 and verify the "cat eyes" pattern as shown in Figure 12. The smaller of the two "eyes" should not be less than 75% amplitude of the other. (% = small lobe/larger lobe x 100)

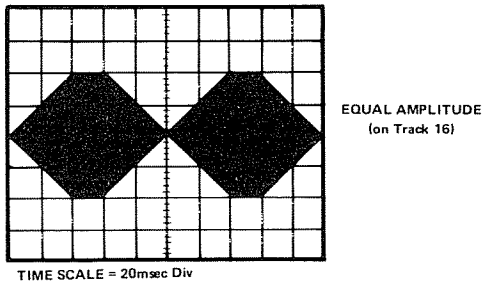
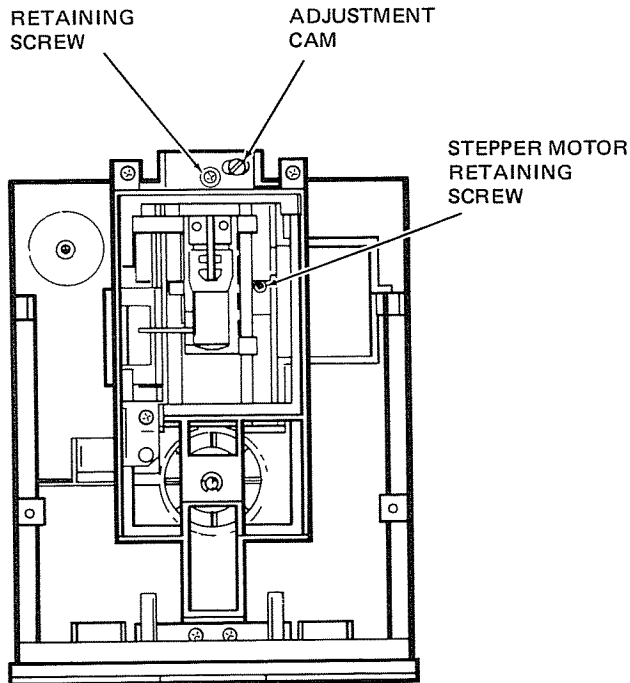


FIGURE 12. "CAT EYES" PATTERN



4. Step to track 00. Return to track 16 and re-verify the pattern.
5. Step to track 34/40 and return to track 16. Re-verify the "cat eyes" pattern

If Radial Needs Adjustment:

- a. Loosen the two retaining screws on back of the unit and the retaining screw on the carriage assembly.
- b. Turn the Adjustment Cam until the "cat eyes" pattern is within 75%. If the pattern does not come within spec, loosen the hex head screw on the collar of the stepper motor and rotate the stepper motor shaft until the "eyes" are to the 75% level. Tighten the hex head screw and return to step a.
- c. Tighten all screws and recheck adjustment.

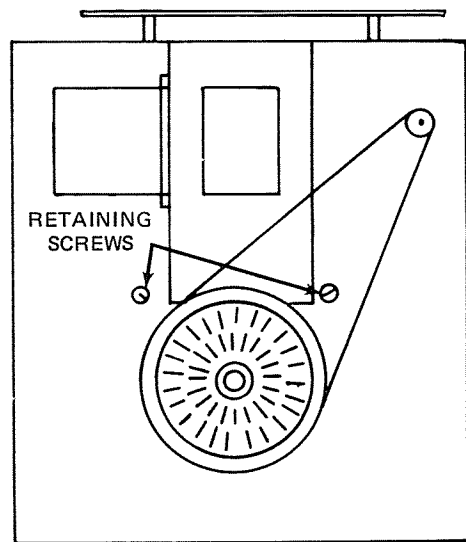


FIGURE 13. RADIAL ADJUSTMENT

Refer to SECTION IV, MAINTENANCE, in the main body of this manual for the two procedures listed below:

J. TRACK 00 ALIGNMENT

K. INDEX SECTOR ADJUSTMENT

L. HEAD AMPLITUDE/COMPLIANCE CHECK

1. Insert a blank diskette and write a pattern to track 34.
2. Set Scope:
Time Base to $10\mu\text{sec}/\text{div}$.
Read the amplitude.
3. Apply an additional 15 grams of pressure to the head load arm. (15 grams is approximately equal to the weight of a 25 cent peice.)
4. Observe the amplitude. If it increases more than 10%, the compliance needs to be adjusted.
5. To adjust the compliance, loosen the two nuts that hold the head load arm in place. While monitoring the amplitude, move the arm until output is highest. Hold the arm in this position and tighten the nuts.
6. Re-verify compliance. If compliance cannot be adjusted properly, replace the head load arm.

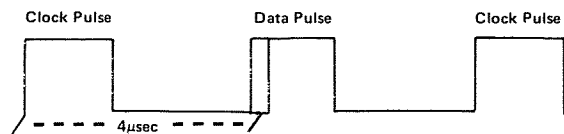
PEAK SHIFT COMPENSATION ADJUSTMENT

R22 is adjusted as follows:

1. With a blank diskette inserted, write a 2F pattern on the innermost track (track 39).
2. Connect the 'scope to TP7 with:

Vert. to 2 volts/div.
Time Base to $1\mu\text{sec}/\text{div}$.
Trigger internal/positive

3. The waveform should look like this:



4. Adjust R22 to center the second pulse between the first and third pulses with a maximum jitter of 240 nanoseconds.

M. FINAL CHECK

1. Use the drive to format and backup a blank diskette.
2. Check the diskette in a known good drive.

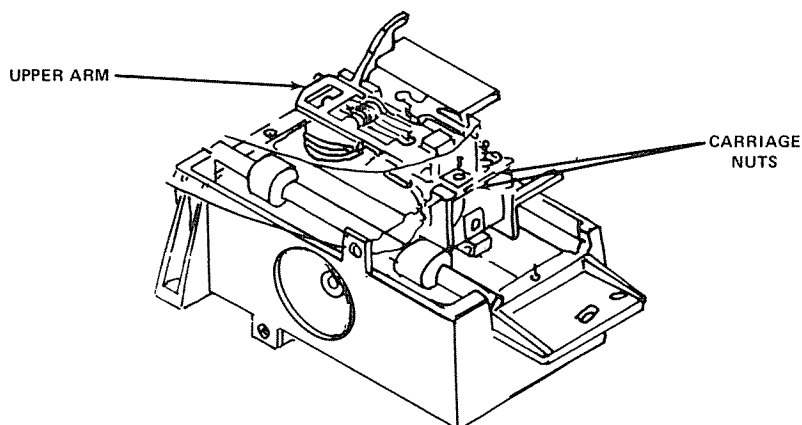


FIGURE 17. UPPER ARM AND CARRIAGE

PARTS LIST
Logic/Servo Controller Board
(Redesign)

| Symbol | Description | Manufacturer's Part Number | Radio Shack Part Number |
|------------|--|----------------------------|-------------------------|
| | PC Board (Rev C) | _____ | 105050-001 |
| CAPACITORS | | | |
| C1 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C2 | 0.1 μ F, 100 VDC, Polyester | ACC302KLG | 250001-233 |
| C3 | 0.1 μ F, 100 VDC, Polyester | ACC302KLG | 250001-233 |
| C4 | Not Used | _____ | _____ |
| C5 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C6 | 0.47 μ F, 50 V, Z5U, Radial | ACC474ZJCP | 250001-647 |
| C7 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C8 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C9 | 0.47 μ F, 50 V, Z5U, Radial | ACC474ZJCP | 250001-647 |
| C10 | 68 pF, 50 V, Radial | ACC680KJCP | 250001-068 |
| C11 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C12 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C13 | 330 pF, 50 V, Radial | ACC331KJCP | 250001-133 |
| C14 | 0.47 μ F, 50 V, Z5U, Radial | ACC474ZJCP | 250001-647 |
| C15 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C16 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C17 | 470 pF, 50 V, Radial | ACC471KJCP | 250001-147 |
| C18 | 3300 pF, 100 V, Polyester | ACC302KLG | 250001-233 |
| C19 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C20 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 251002-410 |
| C21 | 470 pF, 50 V, Radial | ACC471KJCP | 250001-147 |
| C22 | 0.01 μ F, 63 V, Axial | ACC103KJHA | 250102-210 |
| C23 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C24 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C25 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C26 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C27 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C28 | 0.022 μ F, 50 V, Axial | ACC223KJCA | 250002-722 |
| C29 | 0.1 μ F, 100 VDC, Polyester | ACC104JLGP | 251002-610 |
| C30 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C31 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C32 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C33 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C34 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C35 | 100 μ F, 16 V, Electrolytic, Axial | ACC107WDAA | 261002-310 |
| C36 | 100 μ F, 16 V, Electrolytic, Axial | ACC107WDAA | 261002-310 |
| C37 | 10 μ F, 16 V, Electrolytic, Axial | ACC106WDAA | 261002-410 |
| C38 | 0.1 μ F, 50 V, Z5U, Radial | ACC104ZJCF | 250002-610 |
| C39 | 330 pF, 50 V, Radial | ACC331KJCP | 250001-133 |
| CONNECTORS | | | |
| J1 | Header, 5-pin, Right Angle | AJ6815 | 312000-005 |
| J2 | On PC Board | _____ | _____ |
| J3 | Header, 23-pin Right Angle | AJ7049 | 312000-023 |
| J4 | Housing, 4-pin, PC Mount, Power | ART2738 | 313000-004 |
| J5 | Header, 5-pin, Right Angle | AJ6815 | 312000-005 |

PARTS LIST (Cont'd)
Logic/Servo Controller Board
(Redesign)

| Symbol | Description | Manufacturer's Part Number | Radio Shack Part Number |
|---------------------|-------------------------|----------------------------|-------------------------|
| DIODE | | | |
| CR1 | 1N5240B, 10%, Zener | ADX1582 | 600008-001 |
| INDUCTORS | | | |
| L1 | 390 μ H, 10%, Axial | ACA8058 | 461391-010 |
| L2 | 390 μ H, 10%, Axial | ACA8058 | 461391-010 |
| L3 | 5.6 μ H, 10%, Axial | ACA8194 | 461506-010 |
| L4 | 5.6 μ H, Axial | ACA8194 | 461506-010 |
| INTEGRATED CIRCUITS | | | |
| U1 | 74LS123 | AMX3803 | 610002-123 |
| U2 | MC3470 | AMX4467 | 610010-470 |
| U3 | 74LS74 | AMX3558 | 610002-074 |
| U4 | 74LS26 | AMX4522 | 610002-026 |
| U5 | 7438 | AMX3683 | 610002-038 |
| U6 | 74LS11 | AMX3554 | 610002-011 |
| U7 | 74LS86 | AMX3701 | 610002-086 |
| U8 | LM2917 | AMX4181 | 610020-917 |
| U9 | 74LS14 | AMX3716 | 610002-014 |
| U10 | 74LS14 | AMX3716 | 610002-014 |
| U11 | 74LS74 | AMX3558 | 610002-074 |
| U12 | ULN2003A | AMX4513 | 610010-413 |
| RESISTORS | | | |
| R1 | 62 ohms, 1/2 W, 5% | AN0110EFC | 550003-062 |
| R2 | 11 K, 1/4 W, 2% | AN0285CEE | 540300-113 |
| R3 | 24 K, 1/4 W, 2% | AN0526CEE | 540300-243 |
| R4 | 10 K, 1/4 W, 5% | AN0281EEC | 550001-310 |
| R5 | 2.2 K, 1/4 W, 5% | AN0216EEC | 550001-222 |
| R6 | 2.2 K, 1/4 W, 5% | AN0216EEC | 550001-222 |
| R7 | 4.7 K, 1/4 W, 5% | AN0247EEC | 550001-247 |
| R8 | 475 ohms, 1/4 W, 1% | AN0627BEE | 540104-750 |
| R9 | 330 ohms, 1/4 W, 2% | AN0159CEE | 540303-303 |
| R10 | 475 ohms, 1/4 W, 1% | AN0627BEE | 540104-750 |
| R11 | 768 ohms, 1/4 W, 1% | AN0572BEE | 540107-680 |
| R12 | 768 ohms, 1/4 W, 1% | AN0572BEE | 540107-680 |
| R13 | Not Used | | |
| R14 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R17 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R18 | 470 ohms, 1/4 W, 5% | AN0169EEC | 550001-147 |
| R19 | 470 ohms, 1/4 W, 5% | AN0169EEC | 550001-147 |
| R20 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R21 | 1.8 K, 1/4 W, 2% | AN0210CEE | 540300-182 |
| R22 | 50 K, Trimmer, 20% | AP7211 | 560150-302 |
| R23 | 10 K, 1/4 W, 5% | AN0281EEC | 550001-310 |

PARTS LIST (Cont'd)
Logic/Servo Controller Board
(Redesign)

| Symbol | Description | Manufacturer's Part Number | Radio Shack Part Number |
|--------|---------------------|----------------------------|-------------------------|
| R24 | Not Used | | |
| R25 | 10 K, 1/4 W, 5% | AN0281EEC | 550001-310 |
| R26 | 240 ohms, 1/4 W, 5% | AN0151EEC | 550001-124 |
| R27 | 240 ohms, 1/4 W, 5% | AN0151EEC | 550001-124 |
| R28 | Not Used | | |
| R29 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R30 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R31 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R32 | 0 ohms | AJ6814 | 550000-001 |
| R33 | 3.3 K, 1/4 W, 2% | AN0230CEE | 540300-332 |
| R34 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R35 | 150 K, 1/4 W, 2% | AN0384CEE | 540301-503 |
| R36 | 470 ohms, 1/4 W, 5% | AN0169EEC | 550001-147 |
| R37 | 1 M, 1/4 W, 5% | AN0445EEC | 550001-510 |
| R38 | 3.3 K, 1/4 W, 2% | AN0230CEE | 540300-332 |
| R39 | 470 ohms, 1/4 W, 5% | AN0169EEC | 550001-147 |
| R40 | 1 M, 1/4 W, 5% | AN0445EEC | 550001-510 |
| R41 | 10 K, 1/4 W, 5% | AN0281EEC | 550001-310 |
| R42 | 1.5 K, 1/4 W, 5% | AN0206EEC | 550001-215 |
| R43 | 150 ohms, 1/4 W, 5% | AN0384CEE | 540301-503 |
| R44 | 10 ohms, 1/4 W, 5% | AN0063EEC | 550001-010 |
| R45 | 1 ohm, 1/2 W, 5% | AN0022EFC | 550003-001 |
| R46 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R47 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R48 | 2.2 K, 1/4 W, 5% | AN0216EEC | 550001-222 |
| R49 | 1 K, 1/4 W, 5% | AN0196EEC | 550001-210 |
| R50 | 20 K, 1/4 W, 5% | AN0306EEC | 550001-320 |
| R51 | 150 ohms, 6-pin SIP | ARX0241 | 570004-001 |
| R52 | 56 ohms, 1/4 W, 5% | AN0013EEC | 550001-056 |
| R53 | 150 ohms, 1/4 W, 5% | AN0142EEC | 550001-151 |
| R54 | 1 K, Trimmer, 10% | AP7210 | 561501-301 |
| R55 | 2.2 K, 1/4 W, 5% | AN0216EEC | 550001-222 |
| R56 | 150 ohms, 1/4 W, 5% | AN0142EEC | 550001-151 |

TRANSISTORS

| | | | |
|----|---------------|---------|------------|
| Q1 | MPS3906 | AMX3584 | 630007-001 |
| Q2 | MPS3906 | AMX3584 | 630007-001 |
| Q3 | MPS3906 | AMX3584 | 630007-001 |
| Q4 | MPS2907 | AMX4187 | 630008-907 |
| Q5 | 2N5460, FET | AMX4782 | 630006-001 |
| Q6 | 2N5460, FET | AMX4782 | 630006-001 |
| Q7 | TIP110, Power | AMX4331 | 630003-110 |
| Q8 | 2N4124 | AMX4178 | 630002-001 |
| Q9 | 2N4124 | AMX4178 | 630002-001 |

PARTS LIST (Cont'd)
Logic/Servo Controller Board
(Redesign)

| Symbol | Description | Manufacturer's Part Number | Radio Shack Part Number |
|---------------|------------------------------|-------------------------------|----------------------------|
| MISCELLANEOUS | | | |
| TP1 | Staking Pin | AHB9682 | 310024-001 |
| TP2 | Staking Pin | AHB9682 | 310024-001 |
| TP3 | Not Used | _____ | _____ |
| TP4 | Not Used | _____ | _____ |
| TP5 | Staking Pin | AHB9682 | 310024-001 |
| TP11 | Staking Pin | AHB9682 | 310024-001 |
| (Q7) | Heat Sink, TO220 | _____ | 405351-001 |
| (Q7) | Screw, 4-40 x 3/8", Phillips | AHD2249 | 411351-406 |
| (Q7) | Nut, 4-40 | AHD7227 | 410020-001 |
| (R51) | Socket, 6-pin, SIP | AJ7048 | 311500-006 |

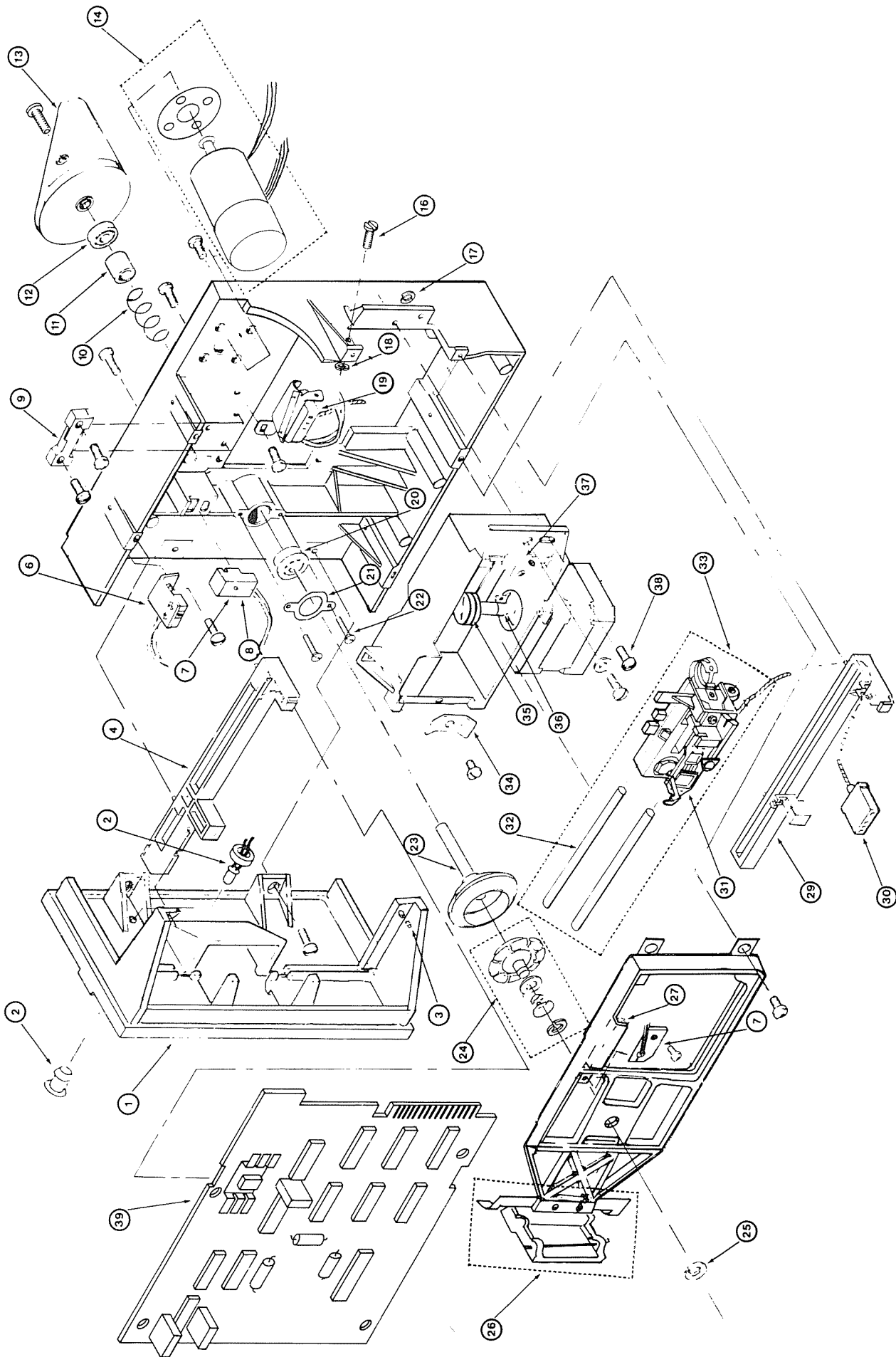
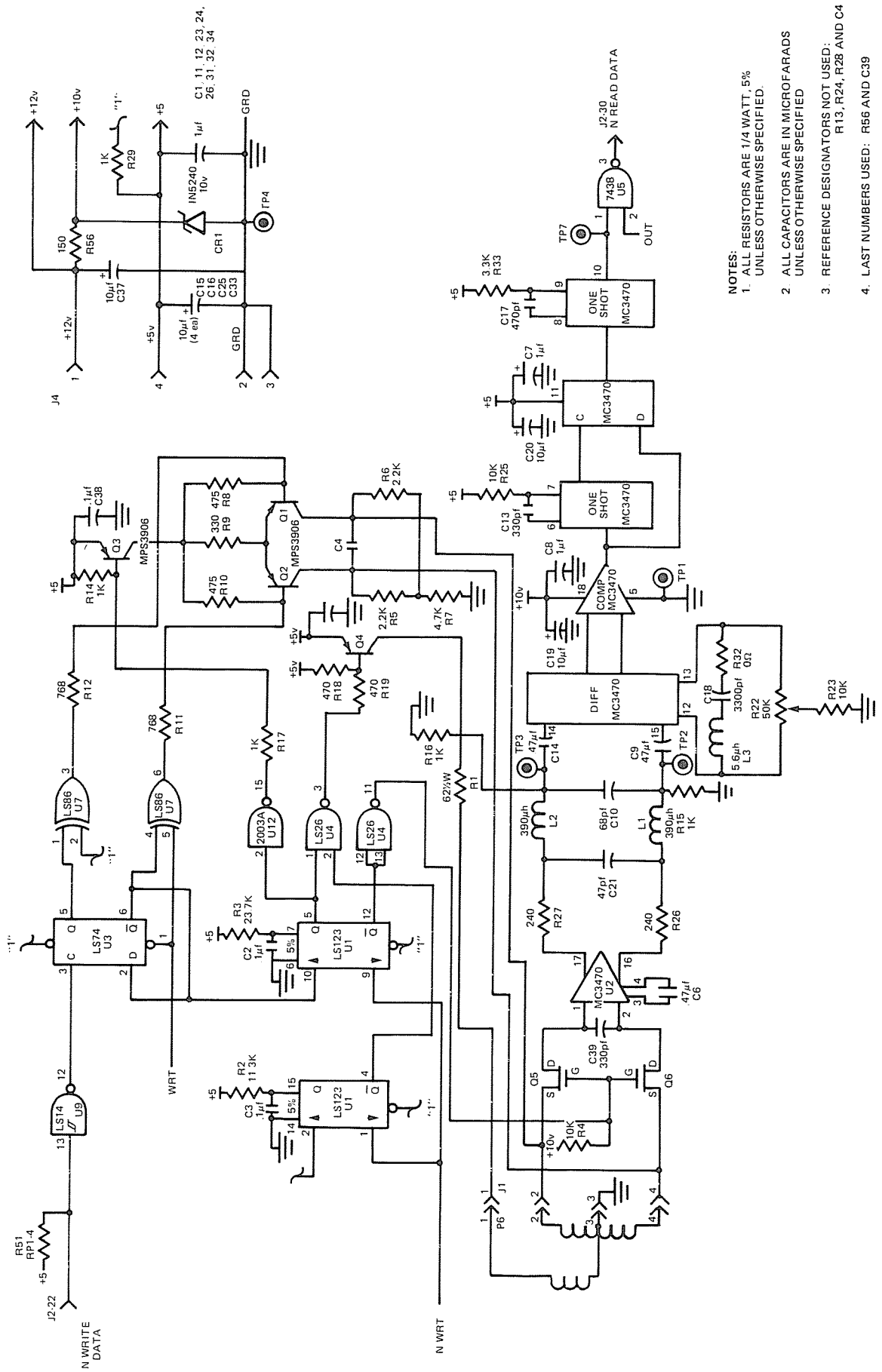


FIGURE 18. ILLUSTRATED PARTS — EXPLODED VIEW

**PARTS LIST
ILLUSTRATED PARTS CATALOG**

| ITEM NUMBER | DESCRIPTION | MANUFACTURER'S PART NUMBER | RADIO SHACK PART NUMBER |
|----------------|--|-------------------------------|----------------------------|
| 1 | Front Panel | 8852025 | AZ5380 |
| 2 | LED Assembly (Panel) | 8852020 | AL1127 |
| 3 | Front Panel Bushing | 8852026 | AHB9684 |
| 4 | Left Hand Guide | 8852024 | ART2743 |
| 6 | Write Protect Switch Assembly | 8852017 | AS2587 |
| 7 | Index Assembly, Type I | 8852019 | ART2739 |
| | Type II* | 8852043 | ART2895 |
| 8 | Detector Holder | 8852048 | ART3003 |
| 9 | Spring Module | _____ | ARB7167 |
| 10 | SSR Spring | 8852060 | ARB6845 |
| 11 | SSR Spring Housing | 8852059 | ART3006 |
| 12 | Lower Bearing | 8852028 | ART2745 |
| 13 | Drive Belt | 8852018 | AB6443 |
| 14 | Drive Motor Assembly | 8852015 | AM4545 |
| 15 | Not Used | _____ | _____ |
| 16 | Track $\emptyset\emptyset$ Screw | 8852057 | AHD1601 |
| 17 | E-ring, large (cam) | 8852049 | AHE0029 |
| 18 | E-ring, small (Track $\emptyset\emptyset$) | 8852051 | AHE0031 |
| 19 | Track $\emptyset\emptyset$ Switch Assembly | 8852016 | AS2586 |
| 20 | Upper Bearing | 8852027 | ART2744 |
| 21 | Hub Retainer | 8852055 | AHB9985 |
| 22 | Hub Retainer Screw | 8852056 | AHD1600 |
| 23 | Machined Hub Assembly | _____ | ART2740 |
| 24 | Cone Assembly (2 pcs.) | 8852021 | ART3511 |
| 25 | E-ring, medium (cone) | 8852050 | AHE0030 |
| 26 | Latch Assembly | 8852022 | ADA0303 |
| 27 | Foam Cone Lever Pad | 8852063 | AHB9986 |
| 29 | Right Hand Guide | 8852023 | ART2742 |
| 30 | Crimp Pin (tin) | 8852045 | AHB9982 |
| | (gold) | 8852046 | AHB9983 |
| | (inside Head Plug) | | |
| 31 | Upper Arm Assembly | 8852044 | ART3002 |
| 32 | Carriage Shaft | 8852065 | ART3050 |
| 33 | Head Carriage Assembly | 8852031 | AH4403 |
| 34 | Shaft Mounting Clamp | 8852064 | AHC0048 |
| 35 | Drive Band, (Stepper) | 8852032 | ART2746 |
| 36 | Collar, (Stepper) | 8852047 | AHB9984 |
| 37 | Track $\emptyset\emptyset$ Stop Kit | 8852052 | ART3004 |
| 38 | Module Cam Screw | 8852058 | AHD1602 |
| 39 | Logic/Servo PC Board | _____ | _____ |
| not shown | Module Cover, clear plastic | 8852062 | ART3007 |
| | Cone Lever Assembly | 8852053 | ART3005 |
| | includes: cone assembly, E-ring, med., latch assembly, and foam cone lever pad | | |
| | Module Assembly SSR | 8852029 | AXX0318 |
| | includes: upper arm assembly, carriage shaft, head carriage assembly, shaft mounting clamp, drive band, collar, track $\emptyset\emptyset$ stop kit, and module cam screw | | |

*Type II Assemblies have a gold band around the photo transistor.



- NOTES:
1. ALL RESISTORS ARE 1/4 WATT, 5% UNLESS OTHERWISE SPECIFIED.
 2. ALL CAPACITORS ARE IN MICROFARADS UNLESS OTHERWISE SPECIFIED
 3. REFERENCE DESIGNATORS NOT USED: R13, R24, R28 AND C4
 4. LAST NUMBERS USED: R56 AND C39

FIGURE 19A. MINI-DISK DRIVE (REDESIGNED) SCHEMATIC DIAGRAM (Sheet 1)

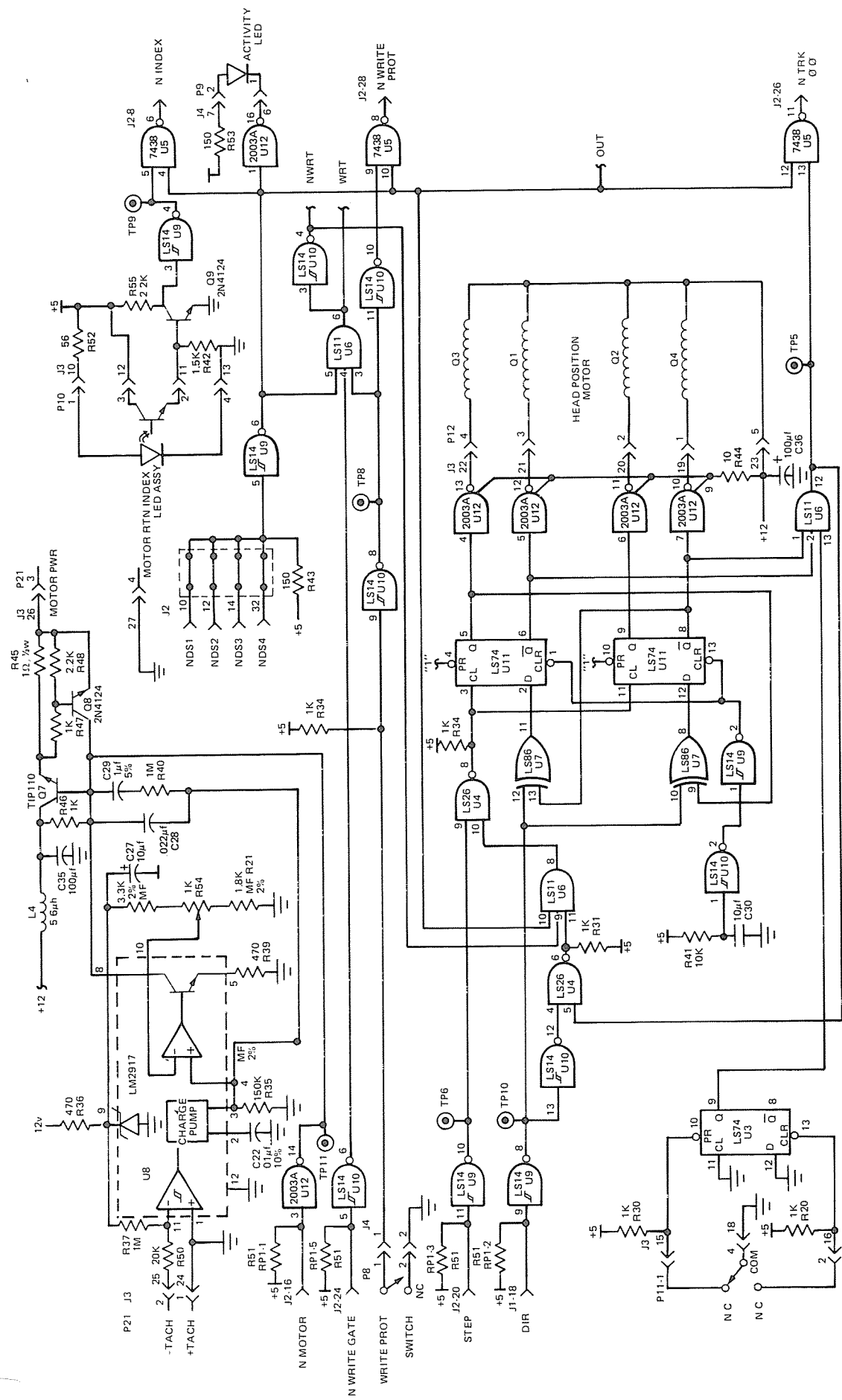


FIGURE 19A. MINI-DISK DRIVE (REDESIGNED) SCHEMATIC DIAGRAM (Sheet 2)

RADIO SHACK A DIVISION OF TANDY CORPORATION

**U.S.A.: FORT WORTH, TEXAS 76102
CANADA: BARRIE, ONTARIO L4M 4W5**

TANDY CORPORATION

AUSTRALIA

**280-316 VICTORIA ROAD
RYDALMERE, N.S.W. 2116**

BELGIUM

**PARC INDUSTRIEL DE NANINNE
5140 NANINNE**

U. K.

**BILSTON ROAD WEDNESBURY
WEST MIDLANDS WS10 7JN**